Poster Session 2
8/1 (四) 11:10-12:10 [一樓展示區]

P2-01 | 論文編號: S0007

12-Bit 5-MS/s Successive Approximation Register Analog-to-Digital Converter with Binary-Scaled Recombination Redundant Capacitor Array

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This paper proposes a 12-bit 5-MS/s successive approximation register (SAR) analog-to-digital converter (ADC) with binary-scaled recombination redundant capacitor array and digital error correction, which is fabricated in the TSMC 90-nm 1P9M CMOS process. The SAR ADC operates with differential inputs to suppress the input noise effectively. The switching process employs a switchback switching algorithm to maintain the common-mode voltage of the comparator and to reduce the comparator dynamic offset. Additionally, binaryscaled recombination is employed in conjunction with a digital error correction circuit to achieve functional calibration. A bridge capacitor is used in the capacitor array not only reduces the number of individual capacitors but also lowers the charging and discharging time of the maximum effective bit. This method reduces the chip area and increases the conversion speed. According to the pre-layout simulation results, the SNDR, SFDR, ENOB, power consumption, and FoM are 69.2 dB, 92.39 dB, 11.2 bits, 264.35 W, and 22.43 fJ/conv.-step, respectively, at the power supply of 1.0 V, an input frequency of 198 kHz, and a sampling rate of 5 MS/s.

P2-02 | 論文編號: S0088

A Current-Squared AOT Buck Converter with Capacitor Current and Inductor Current Sensing Techniques

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This paper introduces a buck converter that utilizes a current squared feedback loop formed by a capacitor current sensor and an inductor current sensor. The proposed converter can achieve high efficiency and fast transient response times. The converter is fabricated with TSMC 0.18μm 1P6M process, and the chip area is 1.15mm ×

1.15mm. The output load current range is 50mA ~ 500mA. The load transient response times are about 1.62 μs and 1.55 μs when the load currents are light to heavy and heavy to light, respectively. The maximum peak efficiency is 94% when the output voltage is 1.5V and the load current is 400mA.
Keyword: capacitance current sensor, adaptive-on-time (AOT), buck converter, current squared modulation.

P2-03 | 論文編號: S0025

A 4.3-5.4GHz 2.65mW Multi-band Ring-VCO-Based Sub-Sampling PLL in 40-nm CMOS Technology for High-speed DDR5.X Applications

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This research will realize a phase-locked loop (PLL) with an output of 4.8-GHz-square-wave and a reference clock of 75-MHz in the 40-nm CMOS technology. In order to mitigate Process-VoltageTemperature (PVT) variations while minimizing circuit area, we designed a multi-band voltage-controlled oscillator based on a ring oscillator. Additionally, the multi-band VCO offers versatility in frequency operation. The proposed PLL exhibits a locking range spanning from 4.3GHz to 5.4GHz through a muti-band selector circuit (MBS). Instead of a traditional PLL, a sub-sampling circuit architecture, direct sampling of the output is performed without going through the frequency divider, preventing the amplification of CP and PFD noise in the locked state, while also eliminating the power consumption of the frequency divider itself. To ensure the proper operation of the PLL, the overall circuit still includes a frequencylocked loop (FLL).

P2-04 | 論文編號: S0130

Defend against flooding attacks on NoC chips with a packet-based defense mechanism

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With the prevalence of System-on-Chip (SoC) or multi-system applications, Network-on-Chip (NoC) has become a popular choice for core connectivity architecture due to its high scalability. However, the strong demand for time to market in chip manufacturing has made the use of third-party IPs in its supply chain a mainstream practice, posing significant security threats to the chips. The impact of these malicious IPs on the system can vary greatly. The impact of thirdparty IPs is significant,

especially in multi-core systems used for applications like neural networks, where hardware such as DRAM or SRAM may need to frequently transmit data. If there are network congestions or other issues hindering data transmission in the periphery, the performance could be severely affected, even rendering the entire chip unable to function properly. This problem can be exploited through the use of Hardware Trojans (HT) to send a large volume of packets to critical components, a technique known as flooding attack. Therefore, in this paper, we propose a defense method against flooding attacks called the packet-based defense mechanism. This method involves authenticating packets at the Network Interface (NI) when they are being packaged. If a packet fails to pass authentication, it will be discarded and prevented from entering the router and the entire network. This approach effectively reduces the number of malicious packets transmitted into the network, while allowing legitimate packets to proceed smoothly without the need to change mapping methods to accommodate HT. Thus, it ensures both the transmission speed and security of the entire network. The experimental results primarily demonstrate the effectiveness of the proposed method in controlling the number of malicious packets entering the network and mitigating the additional execution time caused by HT. For different numbers of HT, the proposed method reduces the number of additional execution cycles caused by HT by 91.93%, and it reduces the number of malicious packets flowing into the network by 72.77%

P2-05 | 論文編號: S0040

An Efficient Co-Processor Design for Cosine Distance Calculation Targeting at Multiple Object Tracking

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The varying number of objects under tracking leads to variable-size cost matrix in cosine distance (CosD) calculation for multiple object tracking (MOT). Hence, a flexible VLSI architecture which can be dynamically configured to compute variable-size CosD cost matrix is inevitable. In this paper, we propose an efficient co-processor design for computing the CosD required in MOT deep learning model. The proposed design has been developed based on the design concept of programmable processors to provide the flexibility in dynamically configuring the hardware. We optimize the proposed co-processor design in the computational complexity through exploiting the techniques of CosD formula transformation, common dot-product sharing, subtraction-based division, adaptive similarity assessment mechanism, and vector dimension and word-length elaboration. These optimizations enable this design to

operate at succinct area cost and low power consumption. In addition, the proposed co-processor design possesses the feature of energy-aware design flexibility allowing the trade-off of lower energy consumption with less demand of data precision. The implementation results show that the proposed design costs about 4065 gates, and obtains a 6.24x performance improvement over the state-of-the-art ASIC design. Additionally, when compared with the state-of-the-art processor, ARM Cortex-A57, the proposed CosD co-processor achieves a 7.27x speed increase. Index Terms—Cosine distance, co-processor, deep learning, multiple object tracking.

P2-06 | 論文編號: S0094

Dynamic Processing Element Optimization in Tile-grained Pipelined Convolutional Neural Network Accelerator

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This paper introduces a flexible hardware architecture for an array accelerator capable of runtime-configurable operation. It optimizes hardware acceleration of 3x3 Convolution operation by dynamically switching between 1-stage and 2-stage architectures based on neural network requirements. The architecture allows for pre-extension of computing units for varying levels of parallelism. It further investigates computational load balance and hardware utilization issue in the 2-stage architecture and proposes a dynamically configurable computational array to optimize overall performance.

P2-07 | 論文編號: S0100

On Environment Context Aware PUF for Environment-Factor Verification Based on Zero Trust

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To counter the rising threats to Internet of Things (IoT) systems, it is crucial to adopt robust security measures that ensure data confidentiality and secure communication. Our research promotes multi-factor authentication based on the zero-trust model, incorporating environmental context as a new verification element. Considering the limited resources of IoT systems, we introduce a novel, lightweight security solution using Physical Unclonable Functions (PUFs). This method exploits the distinct measurement precision of sensors typically found in IoT devices, such as the

temperature sensors analyzed in our study, converting minor measurement discrepancies into regression coefficients for PUF outputs. Moreover, our PUF design can be reconfigured at any time to counteract potential breaches of the current PUF output, thereby enhancing overall security. Implemented on FPGA, our solution is distinguished by its low power consumption and lightweight design. It achieves remarkable results with 49.99% uniqueness, 49.56% unpredictability, and 99.94% reliability. Additionally, it offers a significant 90.12% energy savings compared to earlier models, making it an ideal choice for cost-effective IoT applications.
Keywords: Internet of Things, Sensors, Hardware Security, Physical Unclonable Functions, Regression Model

P2-08 | 論文編號: S0124

Improving LUT-based Threshold Logic Synthesis through Enhanced Area Estimation

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This paper presents a method to improve the stateof-the-art (SOTA) threshold logic synthesis technique which leverages the lookup table (LUT)-based technology mapper for FPGAs. We primarily improve the area estimation of a cut by extending the disjoint support decomposition manager in the covering task. The more accurate area estimation enables the mapper to identify a better covering with reduced area. Experimental results demonstrate that the proposed method achieves an average area reduction of 8.9% compared to the SOTA method, with an insignificant increase in circuit depth. Index Terms—Threshold logic, technology mapping, logic synthesis

P2-09 | 論文編號: S0096

Fast Image-to-Image Technology-Transferable Static IR Drop Prediction Using Machine Learning

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IR drop analysis in the power delivery network (PDN) is crucial for the signoff of integrated circuit (IC) design. Static IR drop significantly affects the IC reliability. Machine learning (ML) has recently been applied to static IR drop prediction works for its high accuracy and efficiency. However, most ML-based static IR drop predictions cannot handle unseen designs and different technologies. These problems incur long training times and data-gathering difficulties, making ML-based methods not applicable in the industry. Therefore, a new methodology for static IR drop predictions is needed. This paper proposes a fast, highly technology-transferable image-to-image ML-based methodology for static IR-drop predictions. To enhance transferability and accuracy, we introduce a new input feature, layerwise maps, which encapsulates the PDN network topology well. We derive a novel generic ML model for various designs and technologies with different numbers of PDN layers. Experimental results demonstrate our methodology's high accuracy, robustness, and technology transferability. For example, we used only 10 circuits to tune our pre-trained model on a new technology and achieved an average error rate of 10.4% IR drop value on unseen circuits. Additionally, we tuned our pre-trained model for the 2023 ICCAD CAD Contest. Compared to the contest winner, our method gets a comparable average error rate of $0.000152mV$ with a run time of less than 1.5 seconds and improves the MAE of the worst case by 29.7%.

P2-10 | 論文編號: S0173

Low Crosstalk Design Techniques for CMOS SPAD Array

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This research aims to improve the crosstalk phenomenon in CMOS single-photon avalanche diode (SPAD) array. It proposes in-pixel circuits to reduce parasitic capacitance at the anode end of SPAD and discusses SPAD structures that effectively reduce crosstalk. This approach reduces the area of on-chip circuits by 59.14% compared to the previous version designed in our laboratory, achieving a fill factor of 17.4% to 26.31% for the SPAD array. Parasitic capacitance is reduced by 4-5 times, and the average current of a single SPAD is reduced by 4-5 times to below 3 μA. Afterpulsing phenomena are also reduced by 3-4 times to below 3%, and with the

isolation provided by the DTI layer, the crosstalk probability is below 0.5%. This design effectively mitigates crosstalk in applications requiring multiple SPAD to be activated in the array.

P2-11 | 論文編號: S0005

Hybrid Energy Harvesting System Using RF and Solar Energies

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This paper proposes a hybrid energy harvesting system that combines radio frequency (RF) and solar energy harvesting into a chip for lowpower devices. The system includes components such as a matching network, rectifier, charge pump, DC combiner, over-voltage protection (OVP), and low-dropout voltage regulator (LDO). The matching network ensures maximum output power delivery to the rectifier, with matching components like capacitors and inductors provided by Murata Manufacturing Company. The power conversion rectifier circuit utilizes a cross-coupled differential drive rectifier circuit to convert RF signals into DC voltage, incorporating boosting functionality. In addition, a solar harvester is employed to provide an additional energy source and stabilize the output by combining it with the RF source using a DC combiner. An over-voltage protection circuit safeguards against high voltage passing from the DC combiner to the LDO. Finally, a low dropout voltage regulator is introduced to produce a stable output voltage. The entire circuit is simulated using the TSMC 0.18-µm 1P6M CMOS standard process provided by the Taiwan Semiconductor Research Institute (TSRI). Simulation results indicate a rectifier conversion efficiency of approximately 41.6%. The proposed RF energy harvesting system can operate with power levels ranging from -1 to 20 dBm, and the rectifier circuit's output voltage is within the range of 1.7-1.8 V. For this research, a 0.2 W monocrystalline silicon solar panel (70×30 mm2) is used, generating 1V. Compared to thin-film and poly-crystalline silicon, mono-crystalline silicon solar panels are utilized. The over-voltage protection circuit limits the voltage to 3.6V when exceeded. The output voltage of the low-dropout linear regulator remains stable at 3.3 V.

P2-12 | 論文編號: S0168

Effective Compute-in-Memory Macros for Enabling Incremental On-Device Learning

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The ability to learn on-device has become a critical factor in successfully deploying edge intelligence applications. However, high data movement during training creates a significant bottleneck for edge devices with limited resources. To alleviate this problem, computein-memory (CIM) is a promising solution. While most CIM-based accelerators focus on inference, effective training on a chip is still a challenge. This work proposes three kinds of CIM macros, CIMI, CIMU, and CIMT, to support training operations efficiently. The experiment based on simulation results shows that we save over 99% backpropagation and weight update time for EMNIST and Cifar10.

P2-13 | 論文編號: S0140

Layer Fusion Pipeline Based Architecture Hardware Accelerator Design

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This paper proposes a hardware architecture and implementation of a Layer Fusion Pipeline. The distinctive feature of this paper is the utilization of Layer Fusion and Pipeline techniques to reduce DRAM access between computations. Through parameterized design, it supports the concatenation of different channel numbers of IFmaps and accommodates various formats for placing data after Convolution operations.

P2-14 | 論文編號: S0120

Analyzing the Impact of Bit-Flip Attacks on Extreme Learning Machines

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This study investigates the impact of bit-flip attacks (BFA) on Extreme Learning Machines (ELM), focusing on the weights of different layers and the significance of individual bit positions within those weights. We employed two strategies: random BFA and indexed random BFA. These attacks are used to assess how they affect the accuracy of the ELM model. By analyzing the influence of each bit position within the weights, we aim to identify which bits are most susceptible to causing performance degradation. The findings of this study present, for the first time, the

specific impacts of BFA on ELM performance at both the layer and bit levels. These results highlight the necessity of establishing robust metrics to effectively assess attack risks and test the efficacy of defense strategies.

P2-15 | 論文編號: S0060

A 6 GHz Upconverter for Quantum Computing

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This paper presents a 6 GHz upconverter for quantum computing. The upconverter consists of a quadrature all-pass filter (QAF), an up-conversion mixer, and an output driver. The QAF is used to generate quadrature signals for the LO input of the mixer. The mixer is based on the Gilbert-cell voltage feedback topology. As the load of the output driver, the transformer achieves the differential-to-single conversion. Consuming the power of 6.3 mW, the upconverter achieves the spurious-free dynamic range (SFDR) of 52 dB for the baseband from 20 MHz to 960 MHz. Fabricated in the 90-nm CMOS process, the upconverter occupies a chip area of 0.79 **mm2** . Index Terms—upconverter, quantum computing, all-passfilter, mixer, Gilbert-cell

P2-16 | 論文編號: S0118

Engineering ASAP7 PDK with Buried Power Rail and Backside Metal Technologies for a Six-Track Standard Cell Library

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The work presented in this paper extends ASAP7 PDK to support buried power rail and backside metal technologies. Because all the power rails are buried inside a bulk, a power distribution network originally deployed above M1 layer now can be deployed with back-side metals which are connected to buried power rails by micro through silicon vias (TSVs). Using these two technologies for designing a six-track standard cell library, we can reduce chip area on average by 13.1%, worst negative slack by 9.4%, total negative slack by 42%, total wire length by 5.8%, and via count by 19.9%. Keywords—standard cell, finFET, buried power rail, backside power distribution network

P2-17 | 論文編號: S0172

ESD protection circuit with dual detection mechanism

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Traditional ESD power-rail clamp circuits play an important role in ESD protection and are widely used in various applications. However, these designs might cause false triggering during fast power-up conditions, potentially turning on the protection circuit and leading to significant current consumption. This could affect the functionality or reliability of the internal circuit. Additionally, the issue of leakage current generated by the circuit cannot be ignored, as it not only leads to unnecessary power consumption but might also affect the operation and reliability of the device. The proposed circuit, designed in a 0.18μm 1.8V CMOS process, incorporates dual detection to provide immunity against false trigger events during fast power-on conditions. Furthermore, it achieves very low leakage current at 125°C.

P2-18 | 論文編號: S0095

Novel Control Scheme for Buck Converters

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In this paper, a novel control scheme for DC-DC buck converter is proposed. The converter uses a dual-loop control method to improve transient performance and does not require a current senor to sense the inductor current. Simulation results shows that the converter can supply 100mA–500mA load current at 1.0V–2.5V output voltage. At the same time, the switching frequency is almost constant, with variations of less than 3%. The recovery time during load transitions is less than 5μs. This paper presents the control scheme, implementation, and simulation results. The converter is designed for the UMC 0.18μm 2P6M CMOS processes. Keywords: adaptive on time (AOT); peak current mode (PCM); current mode control (CMC); voltage mode control (VMC); average current mode (ACM); constant on time (COT)

P2-19 | 論文編號: S0034

Flosit: Float/Posit Coarchitecture Exploiting Value Location in Neural Network

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Posit is the most significant universal number format for compansating for IEEE 754 in both high dynamic range computing and high precision neural network. However, it suffers considerable overhead and time penalty. In this paper, we firstly exploited the value locality of computing data and develop the switching Float/Posit algorithm to save systematic computing time. Secondly, we develop the combined switching architecture, called the Flosit for selecting proper operations efficiently. Thirdly, the Flosit architecture is integrated to further reduce the area and power costs. From prelimianary simulations, the proposed Flosit can automatically have both advantages in speed of Floating-Point and high-dynamic range of Posit

P2-20 | 論文編號: S0157

A Portable EEG-Based Brain Computer Interface for Investigating Bach's Music Effect on Tourette's Syndrome Patients

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This paper presents a cost-effective, noninvasive, portable electroencephalogram (EEG)-based brain-machine interface (BCI) for investigating Bach's music effect on Tourette's Syndrome patients. An EEG recording print circuit board (PCB) is designed and stacked on top of a Raspberry Pi 3 development board, constituting the portable BCI. An experiment was conducted with this BCI to monitor brain wave signals generated by a Tourette's Syndrome patient listening to Bach music and investigate relevant effects. Tourette's Syndrome (TS) is currently considered a neurodevelopmental genetic disorder. Recent research findings address the effect of musical activity on TS patients. Observed musical activities include musical performance, mental imagery of musical performance, and listening to music. The recorded brain waves demonstrate the experiment results that the minor scales likely tend to have a soothing and slowing effect on the TS listener and the major scales are much bolder and cheery. Fastpaced tunes would result in more energy and less relaxation. Slowpaced tunes would result in the opposite. The preliminary experiment results illustrate that Bach's classical music compared with mild pop music leads to more relaxation for the TS patient.

P2-21 | 論文編號: S0174

OnSI-Aware D2D Routing for the Package of Offset-Via and Teardrop

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In recent years,due to the advancements in technology,the use of high-bandwidth memory(HBM) has significantly increased. HBM enables higher memory bandwidth by stacking memory dies on top of each other and using a redistribution layer to transfer the signal to other die. D2D routing thus determines the successful implementation of such HPC systems. Furthermore, we need to take care of offset-via, teardrop and signal integrity required by the advanced packages from customers. We propose multiple-layer RDL routing with fully shielding to deal with essential signal integrity. We found that our D2D routing can reach almost the routing net count upper bound with channel-aware offset-via adjustment method. With the intelligent escape point assignment, we are in no need to consider routing order issue. Results show that our approach can decrease 9% wirelength and 43% layer counts compared with optimized net order based routing in D2D interconnections.

P2-22 | 論文編號: S0108

A Low-Power Open-Loop Charge Steering Amplifier

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This paper improves an existing Open-Loop Charge Steering Amplifier [1] which is for pipelined successive-approximationregister (SAR) analog-to-digital converter (ADC) by designs a new Gain-Boost Circuit. By referring to the Class-AB Operational Transconductance Amplifier structure [2][3] and adopting different output nodes, lower power consumption is achieved while maintaining the characteristics of high gain , high input and output swing. The circuit design of this paper is implemented using United Microelectronics (UMC) 0.18 μm CMOS process. The power supply voltage VDD is 1.8 V. The power consumption is 326 μW which input voltage is 0.71 V.

P2-23 | 論文編號: S0064

Design of Low Power Hybrid DC-DC Buck Converter

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As modern circuits become increasingly complex, the variety of voltages required within these circuits also grows. Consequently, DC-DC converters are gaining more attention, with control over output ripple voltage becoming crucial. This paper proposes using a voltage-controlled oscillator (VCO), a frequency divider, and a phase frequency detector (PFD) to replace operational amplifiers (OP Amps) for detecting the feedback voltage and reference voltage in a DC-DC buck converter. By utilizing different frequencies and phases, the potential difference can be rapidly converged. Additionally, an RLC second-order filter circuit is employed to reduce ripple and improve voltage linearity. Considering the future variability of circuits, multiple subcircuits are used to form the overall circuit. Furthermore, adopting a hybrid voltage detection circuit can mitigate the effects of process variations.

P2-24 | 論文編號: S0058

An FPGA based SoC Convolutional Neural Network Accelerator for End-to-End small-footprint keyword spotting

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Currently, convolutional neural networks have good performance in performing keyword spotting (KWS) tasks. Therefore, in this paper, we training a convolutional neural network for small-footprint keyword spotting and design a SoC neural network accelerator architecture for neural networks. The hardware is implemented on a Xilinx Zynq UltraSacle+MPSoC PYNQ-Z2 FPGA and the results show that the power consumption is 1.336W, recognition time is 200ms when the frequency is 100Hz.
Keywords— convolutional neural network, keyword spotting, SoC design, FPGA

P2-25 | 論文編號: S0154

Eight Channel Analog Front-End Circuitry for the Application of Neural Signal Sensing

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This paper introduces the development and implementation of an Eight-Channel Analog Front-End (ECAFE) circuit specifically designed for the sensing and processing of neural signals. The ECAFE circuit is meticulously engineered to achieve precise neural signal acquisition, boasting high sensitivity and low noise characteristics that are essential for accurate signal interpretation. Comprehensive experimental evaluations have been conducted, and the results robustly demonstrate the ECAFE's efficacy and reliability within the realm of neuroscience research. The advanced design and application of this analog front-end circuitry significantly enhance the performance of neural signal sensing systems. Furthermore, the integration of ECAFE provides substantial technical support for the diagnosis and treatment of neurological disorders, potentially leading to more effective and targeted therapeutic interventions. The findings underscore the ECAFE's pivotal role in advancing neurotechnology and its contribution to the broader field of biomedical engineering. Index Terms—Analog front end, neural signal sensing, capacitive feedback charge amplifier, reconfigurable circuits, powerefficient circuit.

P2-26 | 論文編號: S0063

Design of Low Power Hybrid DC-DC Buck Converter

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As modern circuits become increasingly complex, the variety of voltages required within these circuits also grows. Consequently, DC-DC converters are gaining more attention, with control over output ripple voltage becoming crucial. This paper proposes using a voltage-controlled oscillator (VCO), a frequency divider, and a phase frequency detector (PFD) to replace operational amplifiers (OP Amps) for detecting the feedback voltage and reference voltage in a DC-DC buck converter. By utilizing different frequencies and phases, the potential difference can be rapidly converged. Additionally, an RLC second-order filter circuit is employed to reduce ripple and improve voltage linearity. Considering the future variability of circuits, multiple subcircuits are used to form the overall circuit. Furthermore, adopting a hybrid voltage detection circuit can mitigate the effects of process variations.

P2-27 | 論文編號: S0105

Systematic and Flexible Genetic-Algorithm-Based Feature Reduction for Decision Tree ML-Validation

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In this paper, we propose a systematic geneticalgorithm-based feature reduction method. It has a high design flexibility based on 5-tuple parameter adjustment. The users can decide these 5 parameters to satisfy the demands of making the focus on accuracy or reduced feature amount. The proposed algorithm is verified by decision-tree models with different data sets. As for the data set, ala, the number of features is reduced from 123 to 53 while the accuracy performance has an increase of 4.2%. In addition, for other data sets, the maximum accuracy loss is no more than 3.1% while the feature reduction ratio achieves 41.9%. Its advantage is to provide a design trade-off between accuracy and reduced feature amount. Keywords—feature reduction, genetic algorithm, decision tree, machine learning, training and classification, flexibility.

P2-28 | 論文編號: S0083

The Theoretical Analysis of Convergence and Divergence on Active MOS Sensors of Power Converter by Using HSPICE and HFSS Tools

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This paper tries to study the applications of “Active MOS Sensors” in power conversion circuits, especially in 0.18μm power conversion IC. The reason to apply the active MOS sensors is due to its high- speed performance, when they sensor the voltage or current on the variation of the output regulation line terminals. The higher speed sensing is not only commitment to reduce the sizes of the lumped circuit element, like inductance of inductor; but also provided the integrated of components in the package of power conversion IC, like “current sensors and voltage sensors” without external connection of resistor, capacitor, or others. This action is greatly improvement on noise outside the package of power conversion ICs. The results are clearly to encourage us on the performance of the dynamic response and the cost of external connection action on risk. While it is impossible to having the active MOS sensors that is presented on the performance items all out in perfect, except that limitation of active MOS sensors are well investigated by several outlines based on theoretical expression in applications. Keyword: Active MOS Sensor, Active MOS Current Sensor, Active MOS Voltage Sensor, Higher Speed Settling Time, High Dynamic Response, Power Converter

P2-29 | 論文編號: S0035

SievingNet: An Efficient Pruning Technique for Neural Network

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In approximate computing acceleration of AI neural network, the pruning techniques are usually simple in concept but suffer in efficiency. In this paper, we propose a simple and efficient approximate approach for floating-point multiply-add accumulator during batch forward propagation. During batch forward propagation, the weights of the neural network remain constant and are worthy of approximately converting to ternary-coded binary fixed-point numbers. Then the associated input floating-point numbers are sieved by checking its exponents only. About 20% of inputs are selected for summation. Finally, at least 3 folds of the computation can be sieved out. From practical evaluation, about 70% of realtime can be reduced with an acceptable accuracy loss.

P2-30 | 論文編號: S0072

A New Design of High-Speed Sampler in 0.18μm CMOS Technology

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In this paper, a new architecture of high-speed sampler is proposed. For the increasing demand of high-speed communication systems, a high-speed sampler operated at high frequency is needed. The reset voltage of the proposed sampler is VDD/2 and thus the reset time is shorter. Additionally, the input difference of latch gate is twice larger than the initial input difference which means the positive feedback operates faster and the comparison is faster as well. With these two features, the proposed sampler is nearly twice faster than the typical sampler [1] at same frequency and also can be operated at higher frequency. The new circuit is demonstrated under TSMC 0.18μm CMOS technology.

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BICEP: Exploiting Bitline Inversion for Efficient Operation-Unit-Based Compute-in-Memory Architecture: No Retraining Needed!

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Compute-in-memory (CIM) architecture is promising for its in-situ analog computing ability. However, one practical constraint for CIM architectures is the limited number of activated rows in an operation unit (OU). OU-based CIM architecture only activates a subgroup of memory cells to ensure a large signal margin and sufficient consideration of non-ideal device/circuit effects, which incurs the cost of lowered computing throughput. In short, OU-based CIM architectures suffer from array underutilization to ensure high accuracy. This work proposes a novel architecture, BICEP, which exploits bitline inversion technique to enlarge the OU size without the need to prune, approximate, and retrain. More specifically, this work offers two key contributions: 1) We propose a bitline inversion scheme that guarantees a more than 2× larger OU size without affecting the numerical results and the ADC resolution. The key insight is to selectively apply code inversion on heavy bitlines to constrain their MAC outputs and compensate using low-cost compensation units. We mathematically prove that the proposal can be applied to single- and multi-level cells (SLC and MLC). 2) We propose an inversion-aware weight swapping scheme and weight order propagation. This approach swaps the weight order to maximize the OU size without storage overheads. The extensive experiments on ImageNet classification tasks demonstrate that this work outperforms state-of-the-art OU-based CIM architecture (DL-RSIM) by up to 2.06× speedup and 2.03× energy efficiency.