Poster Sessions

Poster Session 1
7/31 (三) 13:30-15:00 [玫瑰廳]

P1-01 | 論文編號: S0171

ESD Protection Design for the Power Pin in a Negative Voltage Environment

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With the development of process, the gate-oxide of the transistor has become more vulnerable, and electrostatic discharge (ESD) testing has become an important indicator for evaluating the reliability of products. To protect some applications, requiring both positive and negative voltage sources from the ESD damage, the ESD protection circuit should be carefully designed to avoid any unexpected current path under normal operation with the negative voltage. In this article, a power-rail ESD clamp circuit for the power-pin of negative voltage has been proposed and verified in a 0.18-μm 1.8-V CMOS process.
The proposed circuit, realized with only 1.8-V nMOS/pMOS devices, is able to prevent the gate-oxide reliability and latch-up issue under the −5.4-V application. With the proposed ESD detection circuit, the main ESD clamp device, which is a stacked-nMOS (STnMOS), can effectively discharge the ESD current. The STnMOS with a width of 1600 μm can sustain 3.1kV human body model (HBM) ESD stress and perform low standby leakage current of ~8.7 nA at room temperature under the circuit operating condition with −5.4-V supply voltage.Additionally, the proposed circuit maintains leakage current within acceptable limits under long-term powered environments.

P1-02 | 論文編號: S0029

A 12-bit Low Power Successive Approximation Analog-to-Digital Converter With a Wide Input Range

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This paper presents a charge-redistribution successive approximation analog-to-digital converter (SAR ADC) that combines single-sampling capacitors with monotonic switching techniques. It integrates directly with downstream low-voltage components

without the need for additional voltage conversion circuits, allowing operation within a wide input range of up to 5 V. The proposed circuit is implemented using the 180-nm high voltage process, the simulation results yield dynamic parameters SNDR and SFDR of 64.46 dB and 82.21 dB, respectively. The static parameters achieve DNL at -0.667/0.667 LSB, INL at -0.667/0.333 LSB, and FoMw at 31.39 fJ/conversion-step.
Index Term – Analog-to-digital converter (ADC), wide input range, low power, energy efficient, successive-approximation register analog-to-digital converter (SAR ADC).

P1-03 | 論文編號: S0013

A V2 AOT Controlled Buck Converter with Virtual-Inductor-Current-Compensation Techniques

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In recent years, as portable devices have become increasingly trendy, the output capacitor has significantly restricted the size of product applications and impacted the system stability, output voltage stability, and efficiency of the applied converter. As a result, ripple-based constant on-time (RBCOT) control is popular in point-of-load Buck converters due to its fast transient response and improved efficiency under light load conditions. However, it suffers from many problems, such as natural output voltage offset and subharmonic instability. When this control scheme is used in medical devices, frequency variation under different output voltages may cause significant EMI, which is unacceptable for sensitive loads. This paper is designed to provide stable and fixed-frequency output voltage under various load conditions, even with low output RC time constant. The output voltage ripple is about 1 mV in all corners postsimulation.

P1-04 | 論文編號: S0146

A Low Power 24 GHz Single-To-Differential Low Noise Amplifier with Transformer Coupling and Current Reuse Techniques

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A 24-GHz single-to-differential low noise amplifier (LNA) with current-reuse and transformer-coupling techniques is presented for low-power applications. A common source amplifier is stacked on top of the common gate amplifier to generate

differential output and reuse the current. The input and output coupling transformers are employed to achieve higher gain and reduce the chip area. The LNA prototype is designed and implemented in 40-nm CMOS technology with a chip area of 0.79 × 0.62 mm2 . The LNA has a voltage gain of 27.2 dB, NF of 3.9 dB, and IIP3 of –7.5 dBm, while consuming only 1.5 mW from a 1.3-V supply voltage.

P1-05 | 論文編號: S0156

SR-Latch-Based 12T SRAM Cell Design for Low Power Application

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This paper presents a 12T SRAM cell based on SRlatch design concept, which not only eliminates read disturbances and half-select disturbances, but also achievesstable operation in the sub-threshold region. The design uses additional stacked transistors prevent internal data from read disturbances, thereby increasing the RSNM (Read Static Noise Margin) and enhancing read stability. In addition, the proposed design can reduce the power consumption of bit line switching, enabling operation at low voltages. Based on TSMC's 40nm process, the layout of 1-Kb SRAM chip has been implemented and simulation. Its operation voltage is 350mV. When working at 20MHz, the average power consumption is 9.86μW. The average energy consumption saves about 95.05% compared to SE10T[10], and the leakage power consumption saves about 95.4% compared to SE-10T[10].

P1-06 | 論文編號: S0137

Dynamic Reconfigurable Multi-thread AI Accelerator Design

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This paper presents a dynamic reconfigurable multi-threaded AI accelerator designed to enhance computational performance and flexibility by integrating the advantages of reconfigurable computing and multi-thread processing. The architecture supports parallel processing control for four threads, employing dynamic overlapping reconfiguration (DORC) to optimize the overall efficiency of the reconfiguration process. Additionally, the accelerator leverages a stream-based 3-level scheduling to

flexibly map computational streams onto hardware resources, optimizing computational load to achieve optimal hardware performance and improve overall computational efficiency. For different input operation shapes, through PA collaboration, PA can better match the operation shape .Evaluation results indicate that dynamic reconfiguration control significantly enhances the performance of small-scale computational streams, with a maximum execution speed increase of up to 1.3x. Furthermore, the 3-level scheduling mechanism demonstrates the architecture's flexibility, enabling optimal scheduling for maximum computational efficiency.

P1-07 | 論文編號: S0111

Hierarchical Method for Saliency Object Detection Using Block-based Major Color Analysis

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The saliency objects aim to extract the unique area in an image. The most salient regions in the image can be obtained by automatically excluding the background to help quickly find interesting objects for search or focus functions of cameras or other smart devices. The paper proposes a hierarchical method for saliency object detection using block-based major color to accelerate and improve the accuracy of salient objects located on the edges. The experimental results demonstrate that the proposed algorithm in this paper achieves up to 109 frames per second (FPS) under an image with a size of 400300. Compared with previous literature on six publicly available datasets, based on trade-off computing complexity and performance, the proposed algorithm yields outstanding results under the same evaluation criteria.

P1-08 | 論文編號: S0085

Enhancing Semiconductor Testing Accuracy with a Machine Learning-Driven Approach for Probe Card Repair Verification

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This study introduces a machine-learning-based methodology to improve the verification of repaired probe cards in semiconductor wafer testing, leveraging the capabilities of the PRVX 1 system. By integrating advanced machine learning algorithms with machine vision, we develop a model capable of predicting repair quality with a 94% success rate, focusing on electrical and mechanical stability indicators. This approach not only enhances the efficiency of probe card maintenance but also contributes to reducing testing errors and improving the reliability of semiconductor manufacturing processes. Keywords—Wafer Testing, Probe Card Repair, circuit probing, bonded debris, Sensor Data, Machine Learning.

P1-09 | 論文編號: S0161

Recovering Hierarchical Boundaries in a Flat Netlist

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In a typical integrated circuit design flow, a hierarchical design specification is optimized and mapped into a library by a synthesis tool, resulting in a flat netlist without hierarchical instances. However, in some practical scenarios, it may be important to reintroduce into the mapped netlist the boundary of some instances defined in the specification. This paper presents an automated recovery method that works even in those cases when synthesis completely removes the original nodes on the boundary. The paper also discusses several use cases of the recovered boundary in synthesis, verification, and engineering change orders.

P1-10 | 論文編號: S0004

Open-Source EDA Tool of Klayout for CMOS Full-custom VLSI Physical Verification DRC/LVS

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This paper proposes a free and open-source EDA tool of Klayout to implement CMOS full-custom VLSI physical verification for large class teaching. The developed mask layers, DRC, and LVS, allow students to complete projects of mixed-signal integrated circuits. The final project uses a virtual 180nm 1P3M CMOS process to design a 4-bit full-adder circuit as an example to verify its software function operation and environment. Since this EDA software can support various versions of Windows, MAC OS, and Linux systems, students can easily use it in the school computer laboratory and at home.

P1-11 | 論文編號: S0122

A Current-Mode Electrical Stimulator with Charge Balance for Neural Stimulation Applications

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A current mode functional electrical stimulator (FES) with a compensation mechanism is proposed. This eight-channel FES is equipped with a four-bit current DAC to provide adjustable stimulation currents, ranging from 0.5 μA to 60 μA. This research focuses on the development of an electrical stimulator that, by receiving external signals indicating whether to provide stimulation, delivers stimulation-related parameters necessary for nerve stimulation. It generates a bidirectional symmetrical current stimulation waveform to perform functional electrical stimulation. When using traditional constant voltage stimulation, the stimulation effect diminishes as the impedance of the cellular tissue gradually increases. Therefore, the designed electrical stimulator employs a constant current method to ensure that the same level of electrical stimulation effect is continuously maintained. However, due to non-ideal effects of the process, the accumulated charge cannot be completely cancelled by the biphasic current alone. Hence, an innovative class-AB based charge compensator is proposed. Utilizing the characteristics of a class-AB operational transconductance amplifier (OTA), low quiescent current and high compensation efficiency are achieved. Index Terms—current DAC, bi-Phasic stimulation, pushpull amplifier, charge compenstaion

P1-12 | 論文編號: S0166

A Pseudo Jittered Clock Technique for High Speed CMOS DACs

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A technique that exploits a pseudo jittered clock for high speed digital-to-analog converters (DACs), is proposed to suppress spurs and improve the dynamic ranges, especially at high Nyquist zones. DAC output transitions between power levels are one of major factors that cause high order harmonics and mixed unwanted tones. By varying the sampling clock cycle-to-cycle periods of a DAC deliberately, the output signals other than the fundamental tone of the clock will be minimized. To demonstrate the feasibility of the technique, we design an 8-bit 1GS/s current-steering 28nm CMOS DAC with 4-bit digital control delay line and four PRBS generators to explore the performance of the technique. The result shows that mirrored signal magnitudes decline by -10dB/GHz, which suggests the technique is effective and may be adapted with other technique.

P1-13 | 論文編號: S0011

A New Low-EMI Second-Order Delta-Sigma Boost Converter with Transient Accelerated Loops

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This paper proposed a new improved low electromagnetic interference (EMI), fast transient response boost converter with 2nd-order delta-sigma modulation. The proposed second-order delta-sigma modulator converter uses the noiseshaping technique and oversampling theorem to reduce the electromagnetic interference of the output spectrum. And then added the transient acceleration loop to accelerate the transient response also lowers the undershoot and overshoot voltage when the load current changed. The proposed converter has been implemented with T18HVG2, and the chip area is 1.25 × 1.26 mm2 (include PADs). The measured results show that when the output voltage is 1.8V and the load current changes from 10 mA to 100 mA and from 100 mA to 10 mA, the transient responses are 1.1 μs and 1.3 μs, and transient voltages are 19.3 mV and 22.53 mV. Compared to the traditional continuous-time delta-sigmamodulation converter improved 3 μs and 4 μs. The maximum output voltage ripple is 16.2 mV. The output-to-noise ratio (ONR) is 76.05 dB with the sampling frequency of 10 MHz. When the load current is 120 mA and the output

voltage is 1.8 V, the peak efficiency is 90.2%. Index Terms— 2nd-Order Delta-Sigma Modulator, boost Converter, Low EMI, Transient Acceleration

P1-14 | 論文編號: S0158

An All-Digital Delay-Locked Loop with Efficiency Management Design

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The synchronization of clock signals has always been an important issue in a system-on-chip (SoC), affecting whether or not various circuits in the system-on-chip can work harmoniously. In recent years, the demand for mobile devices has increased significantly, and SoC has also been widely used in developing and applying mobile devices. Many circuit functions are integrated into a single chip. However, mobile devices have significantly increased power consumption and size restrictions. Reducing power consumption will be an important issue in mobile devices to increase usage efficiency and prolong product life. Hence, the all-digital delay locking circuit (ADDLL) with fast locking is quite suitable for this type of system. The ADDLL proposed in this paper is simulated under the TSMC CMOS 90nm process. The operating frequency range is 400 MHz ~ 1000MHz, and the locking time is less than 23 cycles. With the high resolution of VDL, the ADDLL locking phase can reach within 0.01 (UI). The circuit power consumption, the JitterPK-PK, and JitterRMS are 0.8 mW, 5.32 ps, and 1.0 ps at 1 GHz and 1 V supply voltage, respectively.

P1-15 | 論文編號: S0065

A Design of Inference Engine for Recurrent Neural Networks with Block-Circulant Weight Matrices Using an FFT-based SoC-FPGA Approach

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In the context of rapidly advancing edge artificial intelligence and limited hardware resources, it is necessary to more ingeniously design and implement recurrent neural network (RNN) inference engines with large weight matrices to improve its efficiency. Previous contents have show the effectiveness of the block-circulant weight matrix approach, which obviously reduces the complexity of each n-dimensional matrix block from a quadratic order O(n 2) to a linear order O(n). This paper presents a design for an RNN inference engine that leverages a co-design

strategy of hardware and software, implemented on an SoC-FPGA platform. In this design, software is responsible for the entire inference process, while the hardware unit conducts individual gate operations of matrix-vector multiplication using the Fast Fourier Transform (FFT) technique. This approach obviously reduces computational complexity from O(n 2) to O(nlogn), further enhancing processing speed. After validation, our proposed RNN inference engine has successfully demonstrated phoneme classification functionality on the TIMIT dataset.
Key words: RNN, LSTM, GRU, accelerator, FFT, FPGA

P1-16 | 論文編號: S00129

Generative Adversarial Network (GAN)-based Spiking Neural Network Training Methodology to Improve Computing Accuracy

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Spiking Neural Networks (SNNs) have been proven as an efficient alternative to mitigate the power consumption issue in traditional Deep Neural Network (DNN) accelerators. In SNN operations, a spike is transmitted from one neuron to another one when the neuron accumulation membrane potential reaches the firing threshold. However, due to the intrinsic features of nondifferential neuron operations, it is difficult to train SNNs efficiently. To address this design challenge, we propose a Generative Adversarial Network (GAN)-based training method to improve SNN training efficiency. This method uses a well-trained ANN model to train the target SNN and determine the optimal spike generation strategy. Compared with the traditional SNN training methods, the proposed GAN-based training method improves computing accuracy by 81.6% to 91.2%. Keywords—Spiking neural network; Adversarial learning method; Spike-Timing-Dependent-Plasticity.

P1-17 | 論文編號: S0155

Enhancing PPG Signal Quality Using a CNN-Based Denoising Autoencoder: Tackling Baseline Drift and Noise Interference

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This study aims to enhance Photoplethysmography (PPG) signal quality using a denoising autoencoder model based on CNN architecture to address noise issues. Cardiovascular diseases are the leading cause of mortality, making wearable PPG devices essential. PPG signals often face noise from baseline drift, muscle artifacts, and power-line interference, leading to misdiagnosis. The proposed model uses 15 encoder and 15 decoder layers with batch normalization to solve gradient vanishing. After post-processing, the average PRD for CBDA decreased to 4.74, and the RMSE dropped to 0.016. These results indicate that post-processing significantly reduces both PRD and RMSE, thereby enhancing diagnostic accuracy.

P1-18 | 論文編號: S0163

LESER-2: Detailed Consideration in Latch Design under Process Migration for Prevention of Single-Event Double-Node Upset

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Single-Event Double-Node Upsets (SEDUs) are increasingly harmful to storage cells as technology nodes shrink below 65nm, rendering conventional RHBD techniques like DICE and TMR ineffective. Recent studies suggest extensive area overhead to protect circuits from SEDUs, leading to inefficiencies. LESER was introduced to eliminate redundant overhead and ensure 100% SEDU tolerance. However, LESER still needs to address spacing impact, dummy gate, and process differences. Thus, LESER-2 was proposed, adopting a two-level architecture (device and circuit level). It replaces the virtual process model with an industrial process model for precise simulations and modifies layouts to protect sensitive node pairs. Experiments show that LESER-2 achieves 100% soft error protection with an average area overhead of 16.5%, resolving all three issues.

P1-19 | 論文編號: S0145

w Bit-Width On-Device Fine-Tuning Framework Tailored for Pretrained Quantized Models

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On-device fine-tuning enables continuous optimization of the quantized model directly on edge devices. This approach reduces the latency of data transferring to a cloud server, enhances privacy by keeping data on the device, and improves adaptability to local environment. To address the issue of limited computational capabilities of edge devices, some low bit-width training methods have emerged. However, none of these methods have addressed the challenge of optimizing a real quantized model, where pretrained quantized models may have varying quantization scales across different quantization blocks. We propose a complete low bit-width on-device finetuning approach for pretrained quantized models, including forward pass, backward pass, and weight update. Experimental results demonstrate that, in VGG-16 transfer learning on CIFAR10, our approach quantizes the forward, backward, and weight update phases of the VGG-16 model all into 8-bit integers. As a result, it achieves a top-1 accuracy of 93.86%, which is comparable to the full-precision baseline, with less than a 0.2% loss in accuracy. This demonstrates that our method can achieve effective performance under low-precision computations for edge devices with limited computational capabilities.
Index Terms—Network quantization, Low bit-width training, On-device training

P1-20 | 論文編號: S0048

Routability-Aware Floorplans with Rectilinear Embedding and Interlocking

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Floorplanning is a critical stage in VLSI physical design, providing early assessments of chip area and routinginduced delays. Traditional floorplanning techniques often impose rigid constraints on block shapes, which may not align well with the flexible nature of soft blocks. This paper explores the construction of rectilinear floorplans under fixed-outline constraints, capable of handling both fixed and soft modules. Our proposed method leverages module embedding and interlocking techniques based on sequence-pair representation and simulated annealing to minimize wirelength. Additionally, Rent's rule is introduced to assess the routability of the resulting

floorplans. Experimental results using MCNC benchmark netlists demonstrate the effectiveness of our methodologies, revealing significant improvements in wirelength reduction compared to existing approaches. These proposed techniques provide increased flexibility and diverse floorplanning options in chip design, effectively enhancing overall design efficiency.

P1-21 | 論文編號: S0121

An Ultra Low Temperature Coefficient Bandgap Voltage Reference with Fully MOS Mirror Mapping Circuitry

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This paper presents a low temperature coefficient bandgap reference (BGR) circuit based on fully MOS and symmetrical offset. By exploiting the complementary characteristics of concave and convex curves, the temperature coefficient is mitigated, resulting in a lower overall temperature coefficient. The achieved temperature coefficient is 18.56 ppm/°C within the temperature range of -20°C to 120°C. The circuit is designed and simulated in the 90 nm standard CMOS process. It consumes 62.79 μW and occupies a layout area of 37.35×87.425 μm2 . A reference voltage of 615 mV is achieved under a 1.2 V power supply.
Keywords: Bandgap Reference Circuit, CMOS, Temperature Coefficient, Band Gap, Mirror Mapping.

P1-22 | 論文編號: S0006

High-Resolution Third-Order Switched-Capacitor Delta-Sigma Modulator

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This paper proposes a feedforward third-order one-bit switchedcapacitor modulator to improve the resolution and remove the noise generated by non-ideal effects in integrated circuits. The feedforward circuit exhibits a good low latency characteristic for the main input signal. By modifying the sampling capacitor of the switched-capacitor integration circuit and utilizing the bootstrapped switch, the high swing of the input signal can be fully integrated into the delta-sigma modulation and the sampling errors generated by the process mismatch effect can be improved. Subsequently, the TSMC 90-nm CMOS process is employed to complete the circuit design and simulation work of the third-order one-bit switched-current deltasigma

modulator. The pre-layout simulation indicates that the signalto-noise ratio (SNR), effective number of bits (ENOB), and power consumption are 96 dB, 15 bits, and 1.3 mW, respectively, at a signal bandwidth of 20 kHz, a supply-voltage of 1.0 V, a sampling frequency of 10.24 MHz, and an oversampling ratio (OSR) of 256.

P1-23 | 論文編號: S0093

An Adaptive On-Time Controlled Buck Converter Using Adaptive Dead-Time Control and Zero Current Detection

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This paper proposed An Adaptive On-Time Controlled Buck Converter Using Adaptive Dead-Time Control and Zero Current Detection, utilizing a zero-current detection circuit enhances efficiency at light loads, while integrating adaptive dead-time control reduces conduction and switching losses, thus elevating conversion efficiency. Ultimately, the switching frequency of the buck converter is stabilized through adaptive on-time control. The proposed converter is fabricated in TSMC 0.35μm Mixed-Signal 2P4M Polycide 3.3/5V processes with a chip area of 1.445×1.445 mm². The switching frequency is designed at 1MHz, and operating with an input voltage of 3.3V, the output voltage remains stable within the range of 1V to 2.4V under load currents ranging from 50mA to 500mA and 500mA to 50mA. Transient response times are measured at 2μs, with undershoot and overshoot voltages recorded at 22mV and 19.6mV, respectively. The peak efficiency is achieved at 94% under a load current of 300mA. Keyword: Buck converter, Adaptive On-Time Control, Zero-Current detection, Transient Acceleration, Integral Current Sensing

P1-24 | 論文編號: S0148

A 0.6, 20Gbps, Low Supply Voltage, Low Process Sensitivity RX Amplifier

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This paper proposes an inverter-based front-end amplifier to improve data rate and power efficiency under low supply voltage. An inverter with a level shifter can achieve high data rates by shifting signal levels beyond the supply voltage levels. The inverterbased differential pair is inserted with a positive feedback inverter to increase

the common-mode rejection ratio (CMRR). Low voltage I/O was very sensitive to supply voltage and process variation. Common-mode feedback (CMFB) and a differential-mode feedback (DMFB) circuit are used to provide a bias level beyond the supply voltage to optimize output level and bandwidth for better quality of the eye diagram. In 40nm COMS process, overall AFE system occupied an active area of 0.0017mm2. under single 0.6V supply voltage, the data rate achieves 20Gbps and total current consumption was 6.64mW. The output eye diagrams reveal 2.2ps (0.044UI) of peak jitter and 0.4V of differential swing.

Keywords—Inverter, Low voltage, Level shift, Receiver

P1-25 | 論文編號: S0143

Optimizing Bearing Remaining Useful Life Prediction through Dynamic Feature Extraction and Time-Attention Model Based on Time-Varying Speed

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Rotating machinery, used in fields like wind turbines and car engines, requires effective maintenance strategies, making RUL (Remaining Useful Life) prediction crucial to reduce costs. Existing methods often ignore time-varying conditions. We propose an RUL prediction method that considers speed variations by selecting robust features, using a self-attention model to focus on valuable features, and applying 1-D convolution and fully connected layers for the final RUL prediction. Our method dynamically adjusts feature selection based on speed variations, reducing root mean square errors from 0.164 to 0.119 compared to related methods.

P1-26 | 論文編號: S0046

Exploiting and Enhancing Computation Latency Variability for High-Performance Time-Domain Computing-in-Memory Neural Network Accelerators

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This work proposed an architecture for a timedomain CIM-based neural network accelerator that leverages the varying output time of the TDC. The key contributions of this work are as follows: 1) We introduce an early-termination scheme for time-

domain CIM, which dynamically determines the length of the CIM clock period by deriving the maximum possible multiply-accumulate (MAC) value based on the current input. This approach reduces computation time for low-MAC results. 2) We propose an input-inversion scheme to decrease the computation time for high-MAC results. By employing linear combination, we perform bit-inversion on large inputs and compensate for the results using a low-cost digital circuit. Experiments show that our schemes could gain 2× ∼ 2.9× speedup under different clock period specifications with 5.82% area overhead compared to the CIM macro. Index Terms—Computing-in-Memory, Time-domain CIM, Neural Network Accelerator, Bit Inversion

P1-27 | 論文編號: S0098

Design and Implementation of a PCA-enhanced CNN for Basal Cell Carcinoma Classification

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This paper designs and implements a two-layer CNN system enhanced by principal component analysis (PCA) for basal cell carcinoma (BCC) classification. BCC is the most common type of skin cancer, requiring extensive medical image analysis, which is time-consuming and subjective. Automated classification systems based on CNNs increase diagnostic speed but require significant computational resources, posing challenges for real-life applications. To address this, we convert the Gabor filters in the convolutional layer of the BCC classification system into transformed filters through PCA to enhance the symmetry of these filters. These enhanced symmetries reduce computational complexity at the algorithm level. Next, we partition the algorithm of BCC classification into software and hardware parts, designing the hardware architecture to meet the system's needs. Experimental results show that our system achieves real-time classification on the CFU-Playground [1] open-source SoC, operating at a clock rate of 54 MHz, improving efficiency, and demonstrating the potential of hardware-software co-design in medical image classification.

P1-28 | 論文編號: S0081

Decomposition Attack on Structure-Based Logic Locking of Reversible Circuits

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With the advancement of technology, the study of reversible circuits for reversible computation has seen rapid growth, leading to emerging hardware security challenges such as intellectual property (IP) piracy, counterfeiting, and reverse engineering. This paper aims to address the vulnerability in RevCLock, the state-of-the-art logic-locking technique for reversible circuits, and proposes an effective attack method to break RevCLock. Our experimental results demonstrate that our proposed attack method can rapidly decrypt circuits locked with RevCLock. Index Terms—Logic locking, Reversible logic, IP piracy, Reverse engineering

P1-29 | 論文編號: S0117

Complexity Reduction Techniques in Compositional Formal Verification for ISA Checking Out-of-Order Processors

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ISA-formal is a formal verification method used to check the ISA of the CPU. To alleviate the state explosion problem of dealing with the out-of-order features of CPUs, we apply abstraction and reduction methods to verify an open 32-bit RISC-V out-of-order superscalar processor named RSD. The processor has two in-order front-end pipelines used to decode and dispatch instructions, 16-entry OoO issue queues used to store instruction information and determine the order of issuing instructions, and five in-order back-end pipelines used to execute instructions and write the result data to register file. This paper employs existing methodologies, such as assume-guarantee reasoning and partial order reduction, to demonstrate the correctness of our proposed abstraction and reduction, which we refer to as “Model Decomposition” and “Architecture Replacement.” Furthermore, we utilize an end-to-end ISA-formal verification approach with splitting properties to shorten verification time. We use a model checker tool to verify the properties against the RV32IM specification of a superscalar out-of-order processor. The result shows that we can get a verified instruction in 775.6 seconds; it saves up to 99.1% of verification time and achieves full proof of ISA checking.

P1-30 | 論文編號: S0087

Automatic Synthesis Flow for Variation-Tolerant Boosted Buffer Circuit from Circuit to Layout

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Manual efforts for trial-and-error adjustments are often required for mixed-signal designs, which could be inefficient for large designs. We present a template-based automated layout flow for low-voltage boosted buffer circuits, which combines designer expertise with the automation program to generate reliable and robust circuits and layouts within minutes. It supports multi-finger layout demand, enabling flexible configuration of transistor structures and automatically merging guard rings for transistors. Experimental results show that the proposed method can quickly generate a design layout that meets design specifications while achieving the expected circuit performance standards.

P1-31 | 論文編號: S0052

A High-Accuracy High-Linearity FPGA Pulse-Shrinking-Based Smart Temperature Sensor

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This paper presents a fully digital smart temperature sensor based on pulse-shrinking mechanism and implemented on field-programmable gate array (FPGA). The proposed design utilizes a pulse-shrinking delay line as the temperature sensing core. As a result, by implementing this approach on an Altera Cyclone IV FPGA 60nm technology, the design achieves a high resolution of 0.053°C over a temperature range of 20°C to 70°C, with a low error range of -0.38°C to 0.42°C without the use of any complex curvature correction. The successful integration of this sensor on an FPGA

platform underscores its adaptability and potential for seamless integration into contemporary VLSI designs, addressing the growing demand for integrated smart temperature sensors capable of ensuring optimal performance and thermal management. Keywords: Pulse-shrinking, field-programmable gate array (FPGA), full-digital sensor, temperature sensor, time-domain.