Oral S14
IC Simulator and Compute-in-Memory

Date/Venue	8/2(五) 10:30-11:30 [玉蘭廳]
Chairs(s)	吳易忠 /國立陽明交通大學電機工程學系 陳勇志 /國立台灣科技大學電機工程系

S14.1 | 10:30-10:41

LithoHoD: A Litho Simulator-Powered Framework for IC Layout Hotspot Detection

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Recent advances in VLSI fabrication technology have led to die shrinkage and increased layout density, creating an urgent demand for advanced hotspot detection techniques. However, by taking an object detection network as the backbone, recent learning-based hotspot detectors learn to recognize only the problematic layout patterns in the training data. This fact makes these hotspot detectors difficult to generalize to real-world scenarios. We propose a novel lithography simulator-powered hotspot detection framework to overcome this difficulty. Our framework integrates a lithography simulator with an object detection backbone, merging the extracted latent features from both the simulator and the object detector via well-designed cross-attention blocks. Consequently, the proposed framework can be used to detect potential hotspot regions based on i) the variation of possible circuit shape deformation estimated by the lithography simulator, and ii) the problematic layout patterns already known. To this end, we utilize RetinaNet with a feature pyramid network as the object detection backbone and leverage LithoNet as the lithography simulator. Extensive experiments demonstrate that our proposed simulator-guided hotspot detection framework outperforms previous state-of-theart methods on real-world data.

S14.2 | 10:42-10:53c

An On-chip High-resolution & High-accuracy Delay Measurement Scheme for TSVs in 3DIC

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This paper presents an on-chip, ring-oscillator (RO) based delay measurement scheme for the through silicon vias (TSVs) of 3DIC. The resolution is very high due to the high sensitivity of the RO period on the subtle change in the RO closed loop delay. In this scheme, each TSV's delay can be accurately derived from the oscillation periods of four closed RO loops. The key idea is to systematically cancel out all gate delays and leave only the routing delays of TSVs. Experimental results on the TSMC 40nm process technology show that the measurement for a TSV's delay can achieve the resolution of a few picoseconds, and the maximum error between our method and SPICE simulation is only 0.19 ps even with process variation considered, which demonstrates the high resolution and high accuracy of our method.

S14.3 | 10:54-11:05

Automated Construction of Equivalent Thermal Impedances of Boundaries for Chip-Level Simulation

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In recent years, with the development of integrated circuits (ICs), the functionality of ICs has been significantly enhanced. However, the increase in power density has led to thermal issues. This paper presents a method to determine the equivalent thermal impedances of boundaries for chip-level simulation and consider system-level effects automatically for improving the efficiency of temperature computation during the design stage.

S14.4 | 11:06-11:17

An Efficient Anomalous Sound Detection by Robust Processing and Reformation of Objective

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Boosted by the Internet of Things (IoT) and neural network (NN), an accurate anomalous sound detection (ASD) system is critical in Industry 4.0 for enabling proactive maintenance. Previous works have enhanced ASD's accuracy by incorporating multi-domain features through advanced NN techniques. However, this often results in significant computational and memory overhead, which

contradicts the IoT scenario. Therefore, we propose a lightweight ASD system by inspecting the core issues. First, to mitigate the noise effect of IoT, we propose dynamic signal processing to stabilize the feature extractor. Second, to adapt to the varying IoT environment, we apply structural learning to enhance the NN's generalization. Additionally, to overcome ASD's data scarcity, we improve the training strategy to strengthen NN's interpretation capability. Finally, compared to the state-of-the-art method on the DCASE 2020 dataset, our approach shows 1.34% accuracy improvement, 16.9% computation reduction, and 43.5% storage reduction.

S14.5 | 11:18-11:29

A 10.2-to-35.6 TOPS/W Compute-In-Memory Design with Reconfigurable Bit Precision and Adaptive Power Adjustment

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In recent years, with the rapid development of Artificial Intelligence (AI), research on reducing the computational power consumption of AI systems has become increasingly urgent. Multiply-accumulate operations (MACs) serve as the core operations in neural network computation, especially in large-scale applications such as Convolutional Neural Networks (CNNs) and Recurrent Neural Networks (RNNs). However, in traditional von Neumann architectures, the separation of the Central Processing Unit (CPU) and memory leads to the problem of transferring a large amount of data from memory to Arithmetic Logic Units (ALUs) when executing MAC operations. This not only increases computation time but also results in significant power consumption. Therefore, this paper proposes a memory-in-computation design that can flexibly adjust energy usage, achieve high energy efficiency, and support multiple operation frequencies. By controlling the switches of each memory row, unnecessary energy consumption is avoided, leading to a reduction in total power consumption by 15% to 60%. Additionally, by adjusting the pulse width, the charging power consumption of capacitors is reduced by 65% per charge cycle. Furthermore, by pipelining the traditional Flash ADC, an average reduction of 47% in ADC computational power consumption is achieved. The proposed design is realized in a standard 28-nm CMOS process. In 8b*8b MAC operations, it can achieve a maximum energy efficiency of 35.6 TOPS/w, surpassing the currently state-of-the-art memory-in-computation circuit chips.