Oral S13
Digital Signal Processing Circuits and Systems

Date/Venue	8/2(五) 10:30-11:30 [薔薇廳]
Chairs(s)	范志鵬 /國立中興大學電機工程學系

S13.1 | 10:30-10:41

Enhancing Multi-Stage Delay Line TDC Data Processing Efficiency with FPGA

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In this study, we were engaged in the development and application of a crucial electronic component, the Time-to-Digital Converter (TDC), within Time-of-Flight Positron Emission Tomography (TOF-PET). The time resolution can reach 6ps, corresponding to a spatial resolution of 1.8mm, which enhances the capability of PET computed tomography images to identify tiny tumor particles down to 0.9mm. The required circuitry is completed using FPGA chips, which can be rapidly assembled and programmed to meet the required resolution performance. Building upon this foundation, the research aims to accelerate data transfer between FPGA chips and computers to facilitate the reception of TDC output data by terminal computers. The hardware of the current project mainly consists of TDC and computers. Matlab software is utilized for convenient visualization of point cloud data. However, TDC data processing in Matlab consumes excessive time, and direct transmission of raw data also consumes too many bus cycles (4 light points/second). This research pre-processes part of the front-end signal within the FPGA chip, enabling reliable transmission of point cloud data directly to the computer. This reduces the frequency of TDC data transmission and eliminates low level noise reduction processing in Matlab. To achieve synchronization with TDC output data, the project utilizes parallel processing structures to accelerate data conversion tasks. Furthermore, registers are deployed within the FPGA chip to accumulate processing results, reducing data transmission frequency and improving data transfer efficiency between TDC and terminal computers for real-time data display purposes. Currently, the data transfer rate of this system can reach 91.74 light points/second. Keyword-TOF PET, TDC, FPGA

S13.2 | 10:42-10:53c

A Compact Electro-tactile System for Braille Display

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Tactile displays have gained significant attention, particularly in the medical field for their application in Braille for the visually impaired. Traditional Braille embossing systems face limitations in terms of device size and complexity due to mechanical stimulation. Therefore, electro-tactile displays have emerged as a promising solution for implementing Braille. Our study presents a compact electro-tactile device with built in electrodes, which is used to determine optimized stimulation parameters. We conducted tests on both polarity and intensity, culminating in a Braille number examination using 0.8mA, 1ms anodal stimulation. The results showed an average accuracy of 64.3% in seven participants, and three of them achieved over 90%.

S13.3 | 10:54-11:05

Efficient VLSI Implementation of Gradient Domain Tone Mapping for Image Enhancement

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This paper presents the development and hardware implementation of a gradient domain tone mapping algorithm for real-time image enhancement. The proposed system leverages an application-specific integrated circuit (ASIC) design, utilizing Taiwan Semiconductor Manufacturing Company's 90nm process technology. The algorithm, based on an optimized local Fattal's operator, enhances image quality by improving contrast, clarity, and detail visibility. Experimental results demonstrate significant improvements in processing speed, chip area, and power consumption, making the system highly suitable for applications in medical imaging, security surveillance, and autonomous driving. The proposed design outperforms existing solutions in terms of efficiency and effectiveness, providing a robust and versatile tool for various high-demand image processing applications.

S13.4 | 11:06-11:17

VLSI Design of a Haze Removal Method Using Color Attenuation Prior and Side Window Filtering

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This paper proposes a haze removal method using the Color Attenuation Prior (CAP) and the concept of side window filtering. To preserve more edges and details of the image, our method uses a side window minimum filter instead of the conventional minimum filter and guided image filter. The

computational complexity of this method will also be lower than that of the conventional CAP-based haze removal method. Moreover, to achieve brighter and more colorful dehazed results, a weighted approach is employed in the calculation of the air light. Our method has been implemented in hardware using TSMC 40- nm technology, with a logic gate count of 19.7K and a working frequency of 667 MHz. This is fast enough to process the 4K (3,840 x 2,160) video at 80 fps.

S13.5 | 11:18-11:29

CRT-based Recursive DFT Hardware Accelerator Design for EIS Impedance Analysis

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Electrochemical impedance spectroscopy (EIS) is a measurement method that indirectly obtains impedance changes based on spectral analysis. Therefore, an efficient and rapid Fourier transform is significant. This study proposes a low-complexity, high-throughput recursive DFT architecture based on the Chinese remainder theorem decomposition method. Compared with previous works or the Goertzel algorithm, this study has the following advantages under a frame size (N) is 5,000: (1) normalized addition operations and multiplication operations save at least 87.5% and 87.5%, respectively, significantly reducing computational complexity; (2) due to the architecture characteristics, the number of single recursions can be reduced to one-eighth, effectively improving computational accuracy; (3) it has eight times the throughput capacity, shortening the transformation time. The proposed architecture is simple and requires only one real multiplier, four real adders, and two constant multipliers from a hardware resource perspective, making it suitable for hardware accelerator designs. This is particularly advantageous for real-time analysis applications in composite sinusoidal stimulation signals or extracting a small number of bins in broadband stimulation signals. In the future, it can also be combined with sensors to realize various EIS application solutions in IoT.