Oral S11

Advanced techniques for logic synthesis and emerging computing

Date/Venue	8/2(五) 10:30-11:30 [桂花廳]
Chairs(s)	黃世旭 /中原大學電子工程學系 陳盈如 /國立成功大學電機工程學系

S11.1 | 10:30-10:41

SMT-based Layout Synthesis for Silicon-based Quantum Computing with Crossbar Architecture

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With the announcement of the most advanced silicon spin quantum-bit (qubit) chip by Intel, silicon-based quantum circuit manufacturing technology has shown the superior potential to realize quantum computing to other technologies because of the mature semiconductor manufacturing technologies and the compatibility with electronics. Due to the bottleneck in scalability caused by interconnections in silicon-based quantum circuits, crossbar architectures serve as one of the most promising solutions for circuitry implementation. This paper proposes the first satisfiability modulo theories (SMT) formulation to optimally solve the layout synthesis problem by simultaneously performing scheduling, mapping, and routing for silicon-based quantum systems with a specific crossbar architecture. The experiments demonstrate that the proposed method can effectively generate layout synthesis results with minimal usage of swap and shuttle gates within the shortest circuit depths, and the solutions greatly outperform those derived from a state-of-the-art work.

S11.2 | 10:42-10:53c

Equivalence Checking of Distributed Quantum Circuits

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Distributed quantum computation is an important and innovative technique in quantum computing, combining multiple quantum computers to enhance the overall computing capacity. Although the synthesis steps for distributed computation are being developed, the equivalence checking aspect is lacking, which prevents us from verifying whether errors are introduced during the synthesis processes. In this work, we extend the previous partial equivalence to a general scenario, which can encompass

distributed quantum circuits. We prove a necessary and sufficient condition for two circuits to be partially equivalent and devise an algorithm for checking the extended partial equivalence relations, addressing a significant gap in quantum program development.

S11.3 | 10:54-11:05

A Neural Network Compiler for ReRAM-Based DNN Accelerators Based on Open-Source TVM

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ReRAM-based DNN accelerators have emerged as a promising solution to address the von Neumann bottleneck. However, achieving design closure for these accelerators requires a comprehensive framework early in the design process. While existing tools can simulate the non-linear effects of ReRAM on hardware behavior, there is a notable gap in high-level design automation tools. In this paper, we introduce a neural network compiler, built on the opensource DNN compiler TVM, to efficiently deploy DNN models onto ReRAM-based accelerators. The proposed neural network compiler employs both model partitioning and layer merging techniques to significantly reduce the amount of data movements in the ReRAMbased DNN accelerators. Experimental data consistently demonstrate that our compiler effectively minimizes data movements across various hardware constraints, facilitating design automation and design space exploration in the early stage of development.

S11.4 | 11:06-11:17

Elevating Boolean Matching to the Word Level

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Boolean matching, a widely employed technique in industrial applications, has conventionally centered on the bit domain. This research addresses a critical gap in the existing literature by extending Boolean matching to accommodate the complexities introduced by modern digital Integrated Circuit (IC) designs featuring datapaths and buses with many input/output ports. Our approach abstracts a gate-level netlist to a word-level expression by reverse engineering techniques and transforms the matching procedure into a Satisfiability Modulo Theories (SMT) problem. Our method may powerfully discover

functional correspondence between two circuits under comparison beyond the standard negation and permutation equivalences of Boolean matching. Experimental results validate the efficacy of our proposed methodology in solving arithmetic benchmarks with extended Boolean matching constraints beyond the capability of standard (bit-level) Boolean matching algorithms. This paper contributes to advancing Boolean matching techniques, providing a valuable framework for handling intricate design elements in contemporary ICs.

S11.5 | 11:18-11:29

DMCGF Dehazing Neural Network Design for Edge-AI Implementation

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In many applications such as autonomous driving, outdoor surveillance, and aerial photography, the haze has become one of the main environmental factors affecting the performance of visual systems. This paper proposes a lightweight dehazing neural network, called DMCGF (Dual Multi-scale Channel Gate Fusion), which includes 4 modules: 1. Multi-scale feature extraction module for capturing local details of haze and the distribution of haze information. 2. Gate fusion block for dynamic weight adjustment fusion and addressing the up-sampling error problem. 3. Feature enhancement module to refine and enhance the fused features, further improving the quality of the dehazed image. 4. Reformulated ASM module to generate dehazed images using the hazy image and the output feature map. From experiments on the RESIDE outdoor dataset with (640×480) images, the proposed DMCGF has the efficient performance with 25.13 PSNR, 0.9401 structural similarity index, 2.204G FLOPs and 0.252M parameters, which are better than the latest works [6, 7, 8]. Also, the DMCGF neural network has been implemented on an Edge-AI platform to achieve 24.3 FPS for real-time applications.