Oral S09
Physical Design Automation

Date/Venue	8/1(四) 11:10-12:10 [薔薇廳]
Chairs(s)	鄭維凱 /中原大學資訊工程學系 陳聿廣 /國立中央大學電機工程學系

S09.1 | 11:10-11:21

IR-aware Multiple Power/Ground Plane Generation on Redistribution Layers in 3D ICs

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In three-dimensional integrated circuits, the interconnection design among chiplets on redistribution layers (RDLs) is crucial for achieving high-performance computing systems. To optimize the inter-chip connections, most of the previous works focused on automatic signal net routing and pin assignment.The power/ground plane generation, is still a manual and time-consuming task, especially when generating the power planes of more than ten power supplies on a limited number of RDLs. This paper proposes a novel Voronoi diagram-based multiple power/ground plane generation methodology that simultaneously optimizes the power/ground planes of all power/ground nets by utilizing the white space of given RDLs, while considering the signal routing blockages, power integrity, and complex design rules. Experimental results show that the proposed approach can achieve not only optimal area utilization but also the best cross-layer power integrity in terms of the total number of redundant vias.

S09.2 | 11:22-11:33

Fast High-Fidelity Warpage Modeling for Advanced Packaging Analysis

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The mismatch of thermal expansion coefficients between different materials incurs nonuniform deformation in a package called warpage. The warpage effect has evolved into a crucial reliability concern that demands careful management in advanced packaging. Considering the severe impact of the effect, we develop an efficient, high-fidelity warpage modeling of preprocessing followed by matrix calculation to address the issue by transforming a three-dimensional packaging structure to a

two-dimensional thermo-solid coupling problem. The transformation provides an efficient measure to reduce the complexity of the packaging analysis. We then apply formal numerical methods to this model for a better trade-off between accuracy and efficiency. Experimental results show that our model averagely achieves respective speedups of 11.0X and 12130X in preprocessing and matrix calculation and an overall speedup of 233.9X with only 1.0% error over the Ansys commercial analysis tool. In particular, such high efficiency and accuracy enable our model for large-scale optimization, simulation, and modeling applications.

S09.3 | 11:34-11:45

Overflow-Aware Via Placement for Dense Die-to-Die Connections in Advanced Package Routing

Hsin-TzuChang,Wen-HaoLiu, IrisHui-RuJiang,Zi-ShengLin,Yueh-HsinTu, andBing-XunSong

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heterogeneous integration, via placement in die-to-die (D2D) package routing becomes a challenging problem. The complex via-related design rules and limited routing resources due to staggered vias make conventional via placement strategies no longer applicable. Poor via placement can significantly degrade the routability and quality of the final routing result. To tackle this challenge, we first model a quadratically constrained quadratic programming (QCQP) formulation for this complex via placement problem. We further propose acceleration techniques to reduce the problem size while maintaining the solution quality. Experimental results show our accelerated QCQP-based algorithm effectively reduces the runtime of the original QCQP formulation and can produce overflow-free routing solutions for benchmarks derived from industrial design in $O(n^{1.53})$ empirical time.

S09.4 | 11:46-11:57

Reinforcement Learning-Based Mixed-Size Placement Prototyping with Semi-Concurrent Optimization

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Placement plays a crucial role in modern chip design, aiming to determine the positions of circuit blocks (macros and standard cells). Traditional data structure-centric heuristics often yield suboptimal placement prototypes, ineffectively guiding downstream mixed-size analytical placement to find the desired results for modern large-scale designs. Recent works have showcased the potential of reinforcement learning (RL) to enhance chip placement by training a policy to place macros as a board game. However, placing macros and fixing them in the earlier stages without sufficient information often incurs undesired solutions. This paper proposes a novel RL-based mixed-size placer with iteratively moving the blocks to characterize dense rewards and comprehensive layout information in each step. We further introduce a semi-concurrent moving mechanism to learn the collaborative dynamics among actions on a subset of blocks at each step. We integrate continuous action spaces to develop a deep Qlearning-based model for learning the semi-concurrent moving policy to derive the proposed moving strategy. Compared with the state-ofthe-art methods, experimental results show that our RL-based placer achieves the best placement quality based on commonly used mixed-size placement benchmarks

S09.5 | 11:58-12:09

A 4.5-Track Standard Cell Library in 7nm Node

Kai-Jie Tong, Wen-Cheng Yang, Ting-An Jian, Bo-Xiang Yang, Meng-Ru Lin, Ming-Yi Huang, Shang-Mou Zhou Shi-Xian Tang, Ya-Zhu Yang, Yi-Jia Wu, Zheng-Jie Peng, Zhong Qing, Yu-Cheng Lin, Rung-Bin Lin
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In this paper we present a 4.5-track standard cell library using ASAP7 PDK extended to support buried-power rails and backside metal wires for power distribution. Besides, the pitches of M4 to M7 are also shrunk to provide more routing resources for a circuit designed with this library. An asymmetric deployment of M2 tracks on the routing fabric is adopted to make best use of M2 routing resources. A multiple-layout approach is employed to enable on-grid pin accesses. For some high-pin count cells or highly routing congested cells, M2 or even M3 pins are deliberately employed to improve pin accessibility. Experimental results show that the 4.5- track cell library is viable. It achieves an average area saving of 18.72%, an average negative slack reduction of 9.18%, and an average total negative slack reduction of 11.97% when compared with the results obtained with a six-track cell library.