Oral S07

Advanced Signal Generators and mmWave Frontend

Date/Venue	8/1(四) 11:10-12:10 [桂花廳]
Chairs(s)	林坤佑/國立台灣大學電機工程學系

S07.1 | 11:10-11:21

An 80-GHz Phase-Locked Loop for Millimeter-Wave Application in 40-nm CMOS

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An 80-GHz charge-pump phase-locked loop (CP-PLL) implemented for mm-wave-band application is presented in this paper using 40-nm CMOS technology. The proposed work adopts a high division ratio frequency division chain. The frequency division chain is composed of two stages of divide-by-2 injection-locked frequency dividers (ILFD), which support a wide locking range, followed by a divide-by2 common-mode-logic divider (CMLD), a divide-by-2 true-singlephase-clock (TSPC) divider and two stages of divide-by-5 CMOS divider. The measured locking range of this PLL is 76.7-83 GHz (7.9%). It consumes 38.3 mW from a 0.9-V supply. The output power is -2.5 dBm. The circuit achieves a reference spur of -51 dBc, an integrated jitter of 355 fs, and the FoM-jitter is -233.2. The core circuit occupies an area of 0.33 mm^2.

S07.2 | 11:22-11:33

A High-frequency Series Feedback Oscillator with Resonator Based on GaN HEMTs

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In this paper, a high-frequency series feedback oscillator with a parallel LC resonator based on 0.15-μm GaN HEMT is proposed. The proposed oscillator utilizes the features of high-power and highfrequency operation of GaN HEMTs and achieves a fundamental oscillation frequency of 49.9 GHz with an output power of 3.2 dBm. Moreover, the frequency can be tuned from 49.4 GHz to 49.9 GHz with a maximum output power of 5 dBm and power variation smaller than 1.8 dB. The PN achieved for the

oscillator is -100.5 dBc/Hz@1 MHz and -130.9 dBc/Hz@10 MHz, respectively. The proposed GaN oscillator has realized the high oscillation frequency based on the 0.15-μm GaN HEMT and achieves the best figure of merit compared with other published V-band GaN oscillators.

S07.3 | 11:34-11:45

A W-band low noise amplifier with coupled-lines in 90-nm CMOS

Yen-Chung Chiang, Ting-Ju Chang and Li-Wu Ku
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This paper presents a W-band low noise amplifier (LNA) design which uses the interstage transmission line-coupled structure in a TSMC 90-nm CMOS process. The proposed circuit adopts a fourstage common-source cascading topology that uses transmission lines as input and output matching components and a source degeneration transmission line at the source of each transistor. At the operating frequency of 78 GHz, the measured gain is 15.72 dB with a noise figure of 4.72 dB. The 3-dB bandwidth of the proposed LNA is 10 GHz, and the measured input P1dB is –14 dBm with an IIP3 of –6 dBm. The power consumption is 22.56 mW under a 1.2-V supply, and the chip area is 581 × 670 μm^2.

S07.4 | 11:46-11:57

6-GHz Sub-Sampling Phase-Locked Loop for Transmon qubit Driver

Jhen-Nong Wu, Chun-Hsuan Fan, Hsiao-Chin Chen

A 6 GHz sub-sampling phase-locked loop (SSPLL) that delivers lowphase-noise microwave signals for qubit control in Transmon quantum computers is presented. The SSPLL is implemented using TSMC 90-nm CMOS technology. The VCO covers the frequency range from 6.155 GHz to 6.279 GHz and achieves the phase noises of -87.81 dBc/Hz at 1 MHz frequency offset and -115.11 dBc/Hz at 10 MHz frequency offset. Consuming the power of 20.1 mW and the chip area of 1.697 $mm2$, the SSPLL with the loop bandwidth of 2 MHz achieves the in-band phase noise of -122 dBc/Hz at 100 KHz frequency offset and the out-band phase noise is -135 dBc/Hz at 10 MHz frequency offset. The frequency noise of the SSPLL is estimated by integrating the phase noise from 2.5 kHz to 2.5 MHz for the quantum gate operation applied with the microwave pluse duration of 20 ns and Rabi frequency of 1 MHz. The SSPLL achieves the frequency noise of 3.6 $kHzrms$ at 300 °K.

S07.5 | 11:58-12:09

A PLL-based Pulse Generator for Test Platform Applications

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This paper describes a 1.97 ps timing resolution pulse generator (PG). The PG adopts the edge combiner (EC) and the phase-locked loop (PLL). The EC can provide an adjusted waveform with a 1.97 ps timing interval. EC adopts the counter scheme and the MOS varactor to define an operational data rate range and a timing resolution. Hence, EC uses the WIN controller to combine the period window with the PLL output. EC also adopts the count-up counter for a wide operational range. The coarse-tuning stage's timing resolution is defined via the PLL period. The fine-tuning stage adopts an autocalibration circuit to arrive at the high-timing resolution for this PG. Thus, the PG can obtain high-accuracy waveforms under the process, voltage and temperature variations. The test chip was implemented in a 90 nm CMOS process. The core area was 215 × 367 μm^2 , and the power consumptions were less than 9 mW. The data rate range of PG was from 2 Mbps to 333 Mbps. PG's timing resolution and average accuracy were 1.97 ps and ±1.18 LSB, respectively.