Oral S05
Power Management ICs

Date/Venue	7/31(三) 15:30-17:00 [海棠廳]
Chairs(s)	范銘彥 /國立成功大學電機工程學系 陳信良 /淡江大學電機工程學系

S05.1 | 15:30-15:41

Development of A 6.78-MHz Wireless Power Transfer System with Transmission Power Regulation

Dao-Han Yao, Tzu-Ning Liu and Po-Hung Chen
National Yang Ming Chiao Tung University

This paper presents a 6.78-MHz wireless power transfer (WPT) system designed for implantable medical devices (IMDs). The proposed resonant current-mode (RCM) regulating rectifier produces two regulated output voltages of 3V and 1.8V through adaptive power control (APC). With transmission power regulation (TPR), the transmitter (TX) transmits proper power to the receiver (RX) to achieve global-loop power control (GLPC), thus enhancing power transfer efficiency (PTE), particularly under light loads. Both TX and RX chips were fabricated using a 0.18-μm CMOS process. With TPR control, a maximum improvement in PTE of 28.2% and a maximum reduction in input power of up to 94.8% can be achieved. The measurement results show a peak RX efficiency of 85.1% and a peak PTE of 31.3%.

S05.2 | 15:42-15:53

A Gate-Sensing Active Driver IC with Delay Compensation for Silicon Carbide Power MOSFETs

Chia-Wei Kuo[1], Ting-Wei Wang[1], Hao-Chung Kuo[2], Chang-Ching Tu[2], Po-Hung Chen[1]
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To permit an optimal tradeoff between current overshoot and switching losses (ELOSS) during the switching on of Silicon Carbide power MOSFETs (SiC), an active gate driver (AGD) IC is proposed in this paper. This AGD IC incorporates a gate-sensing technique without the requirement of external sensing components and adjusts the driving capability during turn-on, thereby suppressing current overshoot, oscillation, and electromagnetic interference (EMI) issues. Additionally, the proposed driver IC compensates for circuit propagation delay to enhance effectiveness in suppressing currentinduced

EMI. The proposed AGD is validated by the 0.18 μm HV BCD process. It achieves a remarkable 40.5% reduction in switching loss compared to the conventional gate driver (CGD) under similar current overshoot conditions. These results underscore the significant advancements the AGD offers in enhancing the efficiency and reliability of SiC-based power management systems.

S05.3 | 15:54-16:05

Fully Synthesizable Digital Low-Dropout Regulator using Low Offset NAND-Based Dynamic Comparator

Chia-Hao Chang, Jia-Wen Yeh, Zhi-Hao Chen and Chien-Hung Tsai
Department of Electrical Engineering National Cheng Kung University

This paper proposes a fully digital synthesized dual-loop lowdropout regulator. By utilizing a comparator-triggered oscillator, the system achieves extremely low quiescent current during steady-state operation, while generating a high-speed operating frequency upon transient arrival to accelerate transient response. Moreover, the dual-loop control composed of Binary search and linear search improves transient response while ensuring loop stability of the system. On the other hand, a low-offset synthesizable dynamic comparator architecture is introduced to further enhance the offset calibration effect of the dynamic comparator by using different offset control units. Additionally, a Complete Design Methodology is proposed to shorten the design time of the DLDO. Design parameters are set according to target specifications using the Design Space, followed by establishing behavioral models to verify system performance. The design is implemented using the TSMC 0.18um 1.8V/3.3V 1P6M Mixed Signal process.

S05.4 | 16:06-16:17

An Environmental Energy Harvesting Interface for Battery-Less Wireless Sensor Nodes

Chi-Wei Liu, Cong-Sheng Huang, Wen-Po Lo and Po-Hung Chen
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This paper introduces a battery-less energy harvesting system for ambient energy using a single-inductor dual-input dual-output (SIDIDO) buck-boost converter. The system generates a regulated output voltage for wireless sensor nodes and achieves high power efficiency with variable input voltage. Unlike previous works that rely on batteries, this system is battery-free. This work not only minimizes quiescent power to 1.9 μW and achieves a peak power conversion efficiency (PCE) of 86.4% using dynamic-power-gating undervoltage lockout (DPG-UVLO), dynamic-voltage-feedback (DVFB), and pulse-frequency modulation (PFM) control.

S05.5 | 16:18-16:29

A 915-MHz Wireless Power Receiver for Battery-Less Electronic Shelf Labels in Biomedical System

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This paper introduces a 915-MHz wireless power receiver designed to power battery-less electronic shelf labels in biomedical systems. The energy harvesting (EH) system comprises an off-chip RF-DC rectifier and a single-inductor single-input dual-output (SISIDO) buck-boost converter. By incorporating an ultra-low-power voltage detector (ULP-VD) circuit, it achieves minimal shutdown power consumption. The system can operate without a battery when the input power exceeds 400 nW, providing 50 mW of output power to electronic shelf labels for brief periods. Furthermore, it reaches a peak power conversion efficiency (PCE) of 84%.

S05.6 | 16:30-16:42

An Adaptive-On-Time Controlled Boost Converter with Current-Mode and Phase-Locked-Loop Techniques

Guo-Yi Jian, Jiann-Jong Chen
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This paper proposed an adaptive-on-time controlled boost converter with current-mode and phase-locked-loop techniques. It utilizes an adaptive on-time controller and adopts new active current sensing circuit and phase-locked loop technique to enhance transient response speed and maintain fixed frequency. This converter was fabricated with TSMC 0.18μm HV 70V G2 process. The chip area is 1.276×1.248mm 2, with an input voltage range of 0.6V-1.2V, an output voltage is 1.8V, and a load current range of 0mA-100mA. It operates at a frequency of 1MHz, and has transient responses of 1.1us and 1us, with amplitudes of 30mV and 35mV, respectively. The maximum efficiency is 90%.

S05.7 | 16:43-16:54

An adaptive On-Time Controlled Buck Converter with Capacitor Current Sensing and Dynamic Slope Compensation

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This paper proposes a capacitor current mode adaptive on-time (AOT) controlled buck converter. Sensing the current on the output capacitor ensures faster recovery to steady-state during load switching by sensing the current on the output capacitor using a capacitor current sensor. In terms of stability, dynamic slope compensation is used to avoid subharmonic oscillations when the duty cycle

exceeds 50%. The converter is fabricated with TSMC 0.18μm 1P6M process, and the chip area is 1.190 mm×1.137 mm. The output load current range is 50~500mA. The load transient response times are approximately 1.73 μs when transitioning from light to heavy load and 3.04 μs when transitioning from heavy to light load. The maximum peak efficiency is 94.89% when the output voltage is 0.8V and the load current is 250 mA.

S05.8 | 16:55-17:06

A Constant On-Time Buck Converter with New Dynamic Slope Compensation Technique using Mismatched Time Constant DCR Current Sensing

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This paper proposes a novel buck converter design that achieves fast transient response and improved loop stability. It utilizes a constant-on-time control circuit and a dynamic slope generator circuit with DCR current sensing. This technique incorporates components with mismatched time constants, enable fast response to changes in load current. The converter was fabricated in a TSMC 0.35μm 2P4M process and occupies an area of 1.471 mm× 1.449 mm. It achieves a peak efficiency of 92.05% at 500mA output current. It operates with a 3.3V input voltage and regulates the output voltage to 2V. The transient recovery times are approximately 1.6 μs and 2.69 μs for light-to-heavy and heavy-tolight load transitions, respectively.