Oral S04

Data and Power Converters

Date/Venue	7/31(三) 15:30-17:00 [桂花廳]
Chairs(s)	張裕鑫 /國立虎尾科技大學電子工程系 陳厚銘 /國立虎尾科技大學電機工程系

S04.1 | 15:30-15:41

A Level-Crossing Hybrid SAR ADC Circuit Design and Verification

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This paper presents a non-uniform sampling levelcrossing (LC) hybrid SAR ADC, designed for biomedical signal sensing. This approach combines the low power consumption benefits of the SAR ADC architecture with the ultra-low power consumption of the LC ADC during steady states, resulting in overall reduced power usage. Additionally, the non-uniform sampling and LC topology contribute to higher linearity, even with a lower resolution ADC.

S04.2 | 15:42-15:53

A 10-bit 10-MS/s SAR ADC with Signal Scaling Technique for Capacitive Touch Sensing System

Yu-Hsien Li, Ming-Yueh Ku, and Shuenn-Yuh Lee
Technique for Capacitive Touch Sensing System

This paper presents a successive-approximation-register analog-to-digital converter (SAR ADC) with a new signal-scaling skill to reduce the output of analog-front-end (AFE) from 5 V signal proportionally to 1.2V without additional external capacitors used. This architecture with split-monotonic CDAC can not only keep the common mode voltage unchanged but also save the power consumption from the capacitor array switch, making this architecture more beneficial for the low power design on a system overview. Simulation results show that this proposed ADC operating at 10 MS/s can achieve a signal-to-noise and distortion ratio (SNDR) of 60.63 dB while consuming 773.75 μW under 5V/1.2V supply voltage, which achieves high energy efficiency and accuracy for the touch sensor system applications.

S04.3 | 15:54-16:05

A Second-Order Noise Shaping SAR ADC with Fully Passive Integrators and Pole Optimization

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This article proposes a new second-order noise-shaping architecture for successive approximation register (SAR) analog-to-digital converters (ADCs), which is a hybrid scheme with capacitor stacking and a multi-input comparator to achieve enough gain in the transfer function. Instead of high-gain comparators and three-path comparators, a two-path multi-input comparator is used in this architecture, which reduces the noise contribution and power consumption. A second-order noise transfer function (NTF) with two zeros at (0.8, 0) and a negative pole at (-0.8, 0) is also implemented, resulting in a better noiseshaping ability compared to the traditional NTF of second-order noise-shaping. This design is fabricated in TSMC 180 nm technology, and the simulation results reveal that the proposed noise-shaping SAR ADC can achieve a signal-to-noise and distortion ratio (SNDR) of 74.15 dB in the bandwidth of 125 kHz. The Schreier figure of merit (FoM) and Walden FoM are 161 dB and 248 fJ/conv.-step.

S04.4 | 16:06-16:17

A 14-Bit 260-kHz BW Second-Order NS SAR ADC with Signal Charge Redistribution Technique

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This paper presents a 14-bit second-order fully passive noise-shaping successive approximation register analog-to-digital converter using capacitors and switches to perform a passive integrator. It employs two prior circuit techniques: embedded passive gain and passive signal residue summation. A circuit technique ofsignal charge redistribution is proposed to reduce the noise and area costs of the comparator and capacitor. Therefore, the zero of the noise transfer function can be improved with an efficient solution. This work achieves SNDR of 87.3dB with a bandwidth of 260kHz at an oversampling ratio of 16. It consumes only 96.6μW of power under a supply voltage of 1V using the 90-nm CMOS technology. The Schreier FoM would reach 182 dB.

S04.5 | 16:18-16:29

An Adaptive On-Time Controlled Buck Converter With Active Gain-Boosted DCR Current Sensing Techniques

Chi-Shu Chen, Yuh-Shyan Hwang, Dong-Shiuh Wu

This paper presents an adaptive on-time controlled buck converter with active gain-boosted DCR current sensing techniques. The proposed converter achieves high efficiency and fast transient response. The proposed converter is fabricated with TSMC 0.18μm 1P6M 3.3V process, and the chip area is 1.2 mm×1.2 mm. The output load current range is 50~700 mA. The load transient response times are about 4.6 μs and 5 μs when the load currents change from 250 mA to 700 mA and from 700 mA to 250 mA, respectively. The maximum peak efficiency is 93.45% when the output voltage is 1.8 V and the load current is 300 mA.

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S04.6 | 16:30-16:42

A Current-Mode Dead-Beat-Controlled Boost Converter with Rail-to-Rail Current-Sensing Techniques

Guan-Zhi Lin, Jiann-Jong Chen

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This paper presents a current-mode dead-beat-controlled boost converter with rail-to-rail current-sensing techniques. The circuit architecture utilizes current-mode dead-beat-controlled, using rail-torail current-sensing technology and dynamic slope compensation technology to achieve the advantages of fast transient response and high stability. This chip is implemented using the TSMC 0.18um HV 1P6M process. The chip area is 1.248×1.226 mm2 . The input voltage range is 0.5V-1V, the output voltage is 1.8V, and the maximum load current is 100mA. The measured result shows the transient response are 1μs and 1μs when the load current changes between 10mA and 100mA, respectively. The peak efficiency is 90.6% under 100mA, with the input voltage of 1V.

S04.7 | 16:43-16:54

A Highly Efficient DC-DC Buck Converter with Overcurrent Protection Circuit

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This paper proposes an over-current protection circuit aimed at enhancing the safety and efficiency of a buck converter. The protection circuit is designed to promptly prevent the buck converter from starting up or shutting it down directly when facing extreme conditions, thus avoiding damage to the power supply unit or to the circuits before and after it. Additionally, a zero current detection device (ZCD) is utilized to improve the efficiency of the synchronous buck converter under light loads. According to simulation results, the input voltage of this buck converter is 3.3V, the output voltage is 1.8V, the overshoot is 16.9mV, the undershoot is 28.0mV, the recovery times are 4.96μs and 5.38μs respectively, and the protected output current is 400mA, the peak efficiency of the load current ranges from 10mA to 300mA is 90%.

S04.8 | 16:55-17:06

A Fast-Transient-Response Delta-Sigma-Modulation Boost Converter With Hysteresis-Voltage Controlled Techniques

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A Fast-Transient-Response Delta-Sigma-Modulation Boost Converter With Hysteresis-Voltage-Controlled Techniques is the circuit that uses a second-order delta-sigma modulation with oversampling and noise shaping techniques to generate a variable switching frequency to break up the output noise and achieve low electromagnetic interference. However, the transient response is relatively slow. The hysteresis-voltage-controller (HVC) circuit then generates an upper and lower voltage VBH and VBL. If the voltage VSense is less than the lower voltage VBL or the voltage VSense is greater than the upper voltage VBH, the power transistors MN and MP are switched on to achieve transient response acceleration. The transient times are all 1.0μs when the load current is varied between 10mA and 100mA, respectively, and the peak conversion efficiency is 88.3% at an output voltage of 1.8V with a load current of 100mA.