Oral S01
Intelligent Sensor Interface Circuits

Date/Venue	7/31(三) 13:30-15:00 [桂花廳]
Chairs(s)	林鴻文 /私立元智大學電機系

S01.1 | 13:30-13:41

A 600-pW, 34.6 ppm/°C, 180 °C Temperature Range CMOS Voltage Reference with Leakage-Based Temperature Compensation and Supply Rejection Enhancement Techniques

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This paper presents a sub-1V output voltage reference circuit using a 0.18-µm CMOS technology. The circuit uses a stacked-diode-MOS-transistor (SDMT) architecture, which ensures excellent supply and temperature independence at low power consumption. Additionally, leakage-based temperature compensation allows for an expanded operating temperature range, while frequency compensation techniques extend the bandwidth of supply rejection. The design achieves a temperature coefficient of 34.6 ppm/°C over a range of -50 to 130 °C, a line sensitivity of 0.014 %/V, and a power supply rejection ratio of -67 dB at 100 Hz. The circuit consumes only 600 pW of power and takes up a chip area of 0.0079 mm^2 .

S01.2 | 13:42-13:53

An ADC Driver With Self-Adaptive Supply Current

Wei-Zhi Lai, Zu-Jia Lo, Tzu-Heng Hsu, Hsiu-Min Yang, Xiu-Zhu Li, Ren-Yong Hung, Yun-Jie Huang, Sheng-Yu Peng
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This paper presents a power-efficient autonomous current adaptation input driver (ACAID) for analog-to-digital converters (ADCs) using floating-gate transistors for reconfigurability. The ACAID autonomously adjusts the supply current during the tracking phase, achieving a high slew rate, and reduces the current during the RC-settling or hold phase to the original low quiescent level. The required sensing and actuating circuits for current adaptation are inherent in the capacitive feedback topology. A prototype version of the ACAID was designed and fabricated in a 0.35 µm CMOS process, achieving −70.1 dB THD with a 100 kHz input signal with 2.8Vpp and 9.1 effective number of bits

(ENoB) near the Nyquist rate with a 200 kHz sampling rate. The proposed ACAID achieves significant power savings at higher input frequencies or reduced tracking periods, with up to 76.2% power savings at a 1MHz sampling rate

S01.3 | 13:54-14:05

A thermal sensor with enhanced accuracy utilizing a new digital calibration algorithm in 12nm CMOS technology

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This paper presents an accurate thermal sensor with a new digital calibration algorithm in a 12 nm CMOS process. The algorithm uses environmental temperature as a reference to mitigate process variations, calibrating BJT |VBE| errors by comparing differences between two devices. The sensor, consisting of a bipolar core, a bandgap reference, and a 10-bit SAR ADC, shows an inaccuracy range of -2.09°C to 1.50°C from 0°C to 80°C without device trimming.

S01.4 | 14:06-14:17

Design of CMOS Capacitively-Coupled Analog Front-End Amplifier for Electrocardiography (ECG) Monitoring

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This paper presents design of a Capacitively-Coupled Instrumentation Amplifier (CCIA) intended for detecting ECG signals ranging from microvolts to millivolts. Considering the Electrode DC Offset caused by the mismatch between the electrodes, this circuit uses a capacitive coupling and capacitor-resistor (using pseudo resistor) feedback structure to form an AC-coupled amplifier while filtering out the DC signal and providing a high-pass corner to eliminate the DC offset. Since the amplitude of the ECG signal varies, making detection more challenging, with a signal amplitude range of approximately 40μV to 5mV, this circuit adopts an inverter-based input pair structure to achieve higher transconductance which reduces thermal noise effects at the same current level. Considering the impact of noise on the circuit, this design reduces low-frequency flicker noise by increasing the input stage area. Additionally, to address the reduction in input impedance caused by capacitive coupling, a positive feedback loop is employed to enhance the circuit's input impedance. Also, to improve the common-mode rejection ratio for suppressing 60Hz power-line noise, the right-leg driven circuit

(RLD) is adopted in this circuit. The RLD circuit samples the common-mode signal and feeds it back to the body to reduce the common-mode interference. The AFE amplifier circuit was fabricated by TSMC 0.18um CMOS mixed-signal/RF process and operates at a 1.8V DC supply voltage. The measured THD is 0.0076%, input impedance is 4.4 GΩ at 10 Hz, and input-referred noise is 2.152 μVrms. The CMRR of the AFE amplifier with the RLD circuit is 111.97dB @60Hz.

S01.5 | 14:18-14:29

A CMOS-MEMS Pressure Sensor with Integrated Front-End for Chemical Vapor Deposition Systems

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In this paper, a CMOS-MEMS capacitive pressure sensor is designed for low-pressure chemical vapor deposition (LPCVD) systems. A buffer layer is utilized in the proposed pressure transducer to effectively protect the sensing diaphragm from breaking down while maintaining high linearity with a compact dimension. A low-power front-end readout circuit is implemented on the same chip to convert the capacitance variance to digital outputs according to the pressure change in the chemical vapor deposition process, near vacuum in this design. The presented device is fabricated through UMC 0.18μm 1P6M CMOS process, and in-house post-processes. The chip size is 1.5×1.5 mm2. Experimental results show that the sensitivity of 0.655 fF/Pa is realized in the range of 0 – 600 Pa.

S01.6 | 14:30-14:41

A Power-efficient Continuous-time Delta-Sigma Resistor-to-Digital Converter for Humidity Sensing

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This paper presents an energy-efficient resistor-to-digital converter (RDC) to detect a wide range of relative humidity. The proposed RDC leverages a delta-sigma architecture, enabling a high linear readout range while maintaining excellent power efficiency. The design achieves a resolution of 0.2 Ω with a rapid measurement time of 0.3 ms while consuming only 87 μW. The energy efficiency figure of merit (FoM) is 10.12 pJ per measurement.

S01.7 | 14:42-14:53

An Array of SRAM-Based Reconfigurable Cognitive Computation Matrix Chips for Multilayer Neural Network Implementation

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This paper introduces a multi-layer network design that utilizes an array of static random-access memory (SRAM)- based reconfigurable cognitive computation matrices (RCCMs). The multiply-accumulate output currents are transformed into single-ended currents through on-chip analog nonlinear circuits, which implement three widely used activation functions: rectified linear unit (ReLU), radial basis function (RBF), and sigmoid function. The output currents from the RCCMs can either be broadcasted to other RCCMs in voltage mode or summed in current mode. A prototype chip, featuring a 17 × 16 RCCM with 4-bit input and weight resolutions, has been designed and fabricated using a 0.18 μm CMOS process. The measured computational efficiency is 3.6 TOPS/W. Calibration involving 49 mismatch parameters significantly improves computational accuracy, mitigating the effects of process variation. The chip's performance was assessed using the MNIST handwritten digit recognition database by implementing a 3-layer neural network, achieving an accuracy of 91.2%.

S01.8 | 14:53-15:04

A Floating-Gate based Programmable Analog Vector Matrix Multiplier with Non-Linear Activation Function

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This paper introduces a novel programmable computing-in-memory (CIM) circuit featuring a compact analog programmable multi-dimensional vector-matrix multiplier (VMM) based on a proposed floating-gate circuit. The proposed VMM can perform four quadrants real-time multiplications and accumulations within the analog domain. By deploying an array of these circuits, multiple analog currents can serve as input vectors, facilitating vector-matrix multiplication with a weight matrix. The resulting output currents can then be utilized as input currents for other VMMs, enabling the implementation of multi-layer networks. Moreover, the paper explores the integration of two commonly used activation functions (AFs), namely radial basis function (RBF), and logistic functions, which convert multiply-accumulation outputs into single-ended currents representing the computation results. Among various non-volatile memory (NVM) options, the floating-gate architecture stands out

due to its advantages, such as area efficiency, low power consumption, and the ability to retain data stored on the floating-gate for an extended period, even after power interruption. Additionally, the values stored on the floating-gate can be programmed, offering a viable solution to address circuit process mismatches through methods like tunneling or injection of charges onto the floating-gate transistor.